

Multichannel capacitance tomograph for dynamic process imaging

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The Division of Nuclear and Medical Electronics of Warsaw University of Technology is an institution where a capacitance process tomograph was first designed in Poland. The design of this capacitance tomograph, its performance and first results are presented in the paper. The tomograph can operate with one or two probes with up to 32 electrodes altogether. Twelve or sixteen electrode configuration is commonly used and a two times twelve or two times sixteen electrode set up is provided for flowmeter applications. Additionally, the device has functionality of a 16-channel capacitance meter for industrial applications. The tomograph has a novel modular structure. It consists of 16 analogue signal cards, a motherboard and a control module with an analogue to digital converter. The measurement is based on a standard charge – discharge method. The signal card is capable to work both as a transmitter and a receiver during the measurement process. The motherboard provides communication between signal cards and the control module using a custom digital bus. The control module contains a 16-bit analogue to digital converter, a control logic, and a serial communication interface. All digital electronic circuits have been designed using programmable logic devices (PLDs).

Keywords: capacitance measurement, capacitance tomography, measurement system.

1. Introduction

Electrical capacitance tomography (ECT) is a useful tool for dynamic processes imaging in research and industry. Capacitance tomography provides three-dimensional information about the process. This knowledge enables improved monitoring and control of the processes. Capacitance tomography is one of the techniques, which have been primary developed for the process technology. It is low cost, high speed, robust and non-invasive. Electrical capacitance tomography is a technique, which aims to image electrical permittivity distribution in a volume enclosed in measuring electrodes.

The paper describes an ET2 capacitance tomograph designed and developed at the laboratory of the Institute of Radioelectronics. The tomograph was elaborated in collaboration with the Industrial Institute of Organic Chemistry and will be used for research works performed by that institute.

Like other ECT systems, the ET2 consists of three units, a sensor, a sensing electronics, and a computer. The ET2 system can work with 8-, 12-, 16- or 32- electrode capacitance probe. The measurement and processing module is an electronic circuitry, containing a set of PCB boards, installed in a separate housing (19-inch wide “Eurocase”), together with a dedicated power supplier and a communi-

cation port. A PC-compatible computer controls a measurement process, provides image reconstruction, presentation, and interpretation.

2. Overview of the hardware part

The electronics employs a standard “charge–discharge” principle of operation. The system has a novel modular structure. Every electrode has a dedicated signal card, with the whole system containing totally 16 PCBs for up to 16 electrodes. During the measurement process, every electrode dynamically changes its role from an active (source) electrode to a passive (detector) electrode. The electrode’s signal card is reconfigured accordingly in real time. All signal cards, as well as the control module are installed on the motherboard.

2.1. Motherboard

The motherboard is a relatively large (16 inch wide), 4-layer printed circuit board (PCB) with mostly passive circuitry and connectors for other electronic units. It contains 32 coaxial connectors (Radiall) for maximum of 32 electrodes. All electrodes are connected with the motherboard via intermediate coaxial connectors on the front panel. The electrodes are connected to the signal cards, 2 electrodes per card. The motherboard contains also 8 PLDs (Altera EPM7064AETC44) and connectors (Phoenixcontact “Mini

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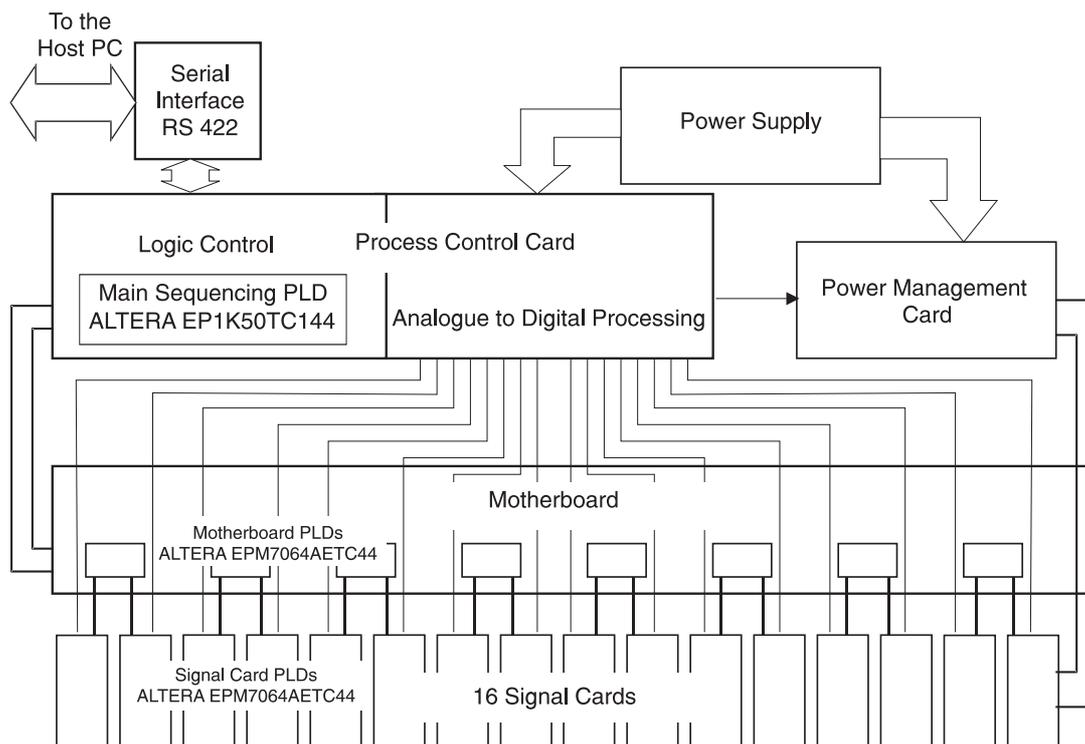


Fig. 1. The block diagram of the ET2.

Combicon” series) for all other PCBs in the unit, including the signal cards. The PLDs buffer certain timing signals, decode and select the signal cards. The PLDs have made it possible to limit the number of control signals useful for the whole system by employing a common inter-module digital bus structure on the motherboard. The motherboard contains also a power regulator for its PLDs (Maxim MAX604CSA).

2.2. Signal card

Each of the 16 Signal Cards is a 4-layer PCB with the following main components:

- two ICs with 8 “front end” analogue switches,
- 2 charge amplifiers (1 dual operational amplifier IC),
- a set of analogue multiplexers to control feedback circuits of the amplifiers,
- 1 programmable gain instrumentation amplifier IC,
- 1 PLD (Altera EPM7064AETC44) to interface the card with the inter-module bus on the motherboard,
- a set of voltage regulator chips: ADP3303 +3,3 V regulator for the Altera; LM78L05 and LM79L05 +/-5 V regulators for the ADG612 and LM78L12 and LM79L12 +/-12 V regulators for the rest of analogue circuitry on the signal card.

When in an active mode, every electrode is driven by a square wave generator located on the electrode’s signal card. In a passive mode, the electrode is connected to charge the detection and amplification circuit. The square wave generators employ analogue switches, connected to the +15 V supply and to the ground, to drive

the selected transmitting electrodes with rectangular waveforms.

The front-end analogue switches (ADG612YRU) are primary detection switches used for reception. They feature low charge injection and are powered from low voltage (+/- 5 V) for further reduction of a charge injection effect.

One signal card supports two electrodes. For a receiving electrode, the detection switches are open and closed alternatively, so that capacitance charging and discharging pulses are directed to both charge amplifiers. The unused electrode is disconnected from the amplifiers and shorted to ground.

For transmitting electrode, the square wave generator switches are open and closed alternatively. The electrode is connected alternatively to +15 V and to the ground, so that square wave is generated. The unused switches are open. The low-voltage detection switches are protected against damage from the large amplitude square wave. The unused electrode is also shorted to the ground.

Both charge amplifiers may operate with various feedback configurations, with resistive and capacitive components of the feedback impedance selectable by the analogue multiplexers. The signals from both charge amplifiers are fed to the programmable gain differential amplifier. The four gain values are available ($\times 1$, $\times 2$, $\times 4$, $\times 8$).

2.3. Control module

The control module can be divided into: analogue path, digital control circuit and communication interface. The main digital control device is RAM-based Field Program-

mable Logic Array (FPGA) from Altera. This IC carries out all the essential measuring and communication algorithms, required from the signal card.

2.3.1. Analogue path

Analogue signal from selected Signal Card undergoes analogue preprocessing, shifting, amplifying, and attenuating. Two multiplying, 12-bit DACs type MAX501 (Maxim) work as digitally programmable: shifter and attenuator. The final analogue signal is digitally converted using the AD676 intelligent (auto-calibrating), 16-bit ADC (Analog Devices). The DACs are controlled by the main control FPGA circuit using dedicated an 8-bit bus ADA[0..7]. The ADC's digital side is tied directly to the FPGA.

2.3.2. Digital control circuit

A high integration FPGA device (Altera EP1K50TC144, ACEX series) is used as a main timing and control element. It contains 2880 macrocells, each capable to generate any combinatorial or sequential Boolean function of 4 variables and 10 blocks of versatile, dual-ported memory, 4 kilobits per block. The FPGA employs Static RAM technology; the device thus must be initialised (configured) prior to the work after every power on. The configuration process requires writing into the device a data stream, being a digital representation of the project to be implemented. Serial EEPROM IC (Altera EPC2TC32) is used as a source of the configuration data. The two devices co-operate during every power-on time so that the FPGA is initialised automatically.

2.3.3. Communication interface

The control module contains two independent serial ports of RS-422 and RS-232 standards as the basic interface between the ET2 and PC host. The RS-422 interface employs MAX490 chips, providing Baud Rates up to 2.5 Mega Baud. The RS-232 interface employs MAX3225 chips, providing Baud Rates up to 1 Mega Baud. The RS-232 – compatible interface has a limited range both due to its physical properties and due to the limitations of serial port in popular PCs.

To address extended communication needs, attachment of additional communication interfaces is possible. Solutions such as light-guide link, Ethernet connection, mobile GPRS, or industrial band radio data transmission are obtainable by attaching additional interface daughter cards.

2.4. Power supplies

Switching power regulators (+/-15 V and +5 V) from Traco Power of Switzerland are used as a main power supply for the whole measurement system. Precision analogue circuitry is powered from +/-14 V voltages, obtained from

LM2941/LM2991, digitally switchable linear regulators. The control circuitry takes care of proper sequencing of all the voltages, so that the analogue circuitry is powered on only if the digital control has been fully configured and instructed to perform measurements.

The programmable logical devices are powered from +2.5 V and +3.3 V, obtained from local linear regulators.

3. Data acquisition, image reconstruction and visualization

3.1. Communication protocol

The communication between the tomograph and the computer is performed using serial interface in an asynchronous mode. The default interface configuration is as follows: 115.2 kbaud, 8 data bits, no parity, 1 stop bit. The hardware parity control is not used, instead the software data integrity control is performed.

It is possible to remotely change the number of electrodes serviced, the number of projections and the number of data frames. Measurements are carried out and data frames transmitted continuously with possibility to start and stop data transfer remotely.

3.2. Data acquisition and image reconstruction

The elaborated ET2 program is a multitasking application which allows real time data acquisition and image visualization in the same time.

The ET2 program allows control of the tomograph calibration, data acquisition with on-line image monitoring, image visualization and data storage in different formats. The ET2 software supports various modes of data acquisition with configurable number of electrodes, number of projections for one frame, number of frames in the frame series and sampling time. The sensor calibration is required before the acquisition. The calibration consists of two measurements for the lowest and the highest value of measurement range. During data acquisition, on-line image visualization is performed. The LBP reconstruction algorithm is used for on-line image visualization. The sensitivity matrix is required for LBP reconstruction. The ET2 program uses sensitivity matrix generated by other simulation program. For off-line image reconstruction we plan to use more complicated iterative algorithms. The matrix size of reconstructed image is 3232 pixels (default) or 1616 pixels. The images may be displayed in different colour palettes. The data thresholding (windowing) is available.

The ET2 software employs proprietary data format for acquisition data; however export of projections and image data in additional formats is also possible. The program exports data in a text format. It is also possible to store the image in graphic format as a bitmap.

4. Results

Due to application of modern analogue and digital technology the tomograph has high sensitivity of measurement. The RMS error for 32 channels is less than 0,025% and the difference between channels without any tuning is better than 0.01 (1%) as seen on chart below.

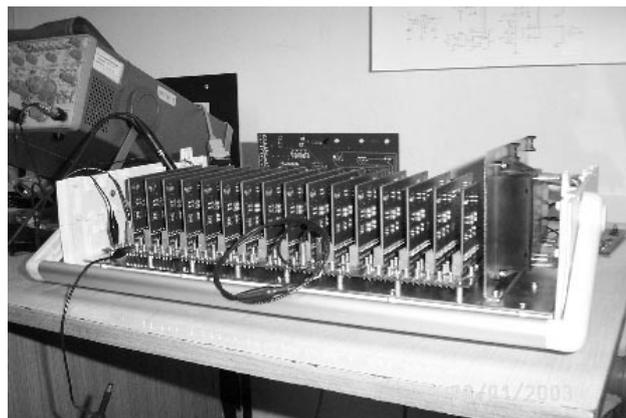
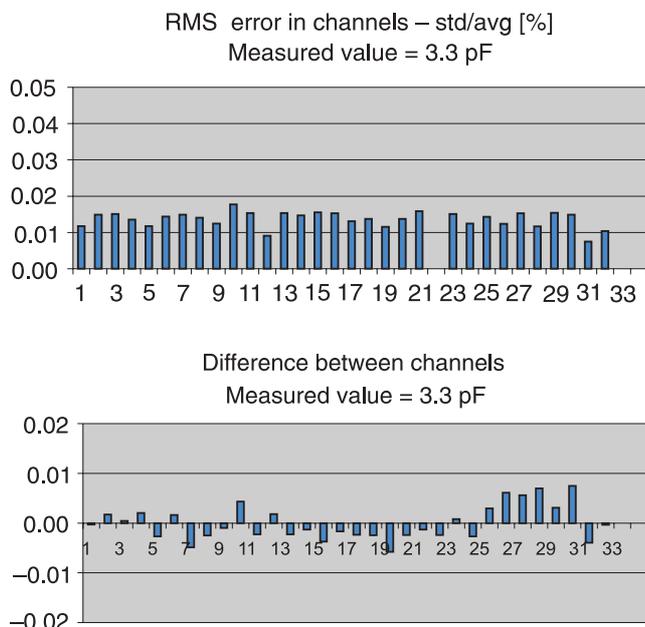


Fig. 2. Capacitance tomograph – ET2.



Fig. 3: Twelve electrode sensor.

After testing the electronics, whole tomographic imaging system was tested. The twelve electrodes sensor was prepared. The sensor was fabricated using copper foil and sewage pipe. The copper foil was glued on outside surface of the sewage pipe. The view of the designed tomograph as well as the sensor has been demonstrated in Figs. 2 and 3.

First tests were done using both static and dynamic objects. Spatial resolution was tested using polypropylene rods (Fig. 4). Image of three polypropylene rods were registered. The images show a clear gap between rods. Imaging of dynamic objects was tested using polypropylene drops and vegetable oil. The images of the oil filling the sensor are presented in Fig. 5. Evaluation of electrical signals has shown that 300 frames per second would be possible.

5. Discussion and future work

The elaborated system is a full feature capacitance tomography imaging system. It can support a sensor with up to 32 electrodes. Measurements with 32, 16, 12, and 8 electrodes are possible. The tomograph has been designed to work also simultaneously with up to 4 planes with 8 electrodes each. The theoretical dynamic acquisition speed of about 300 frames/s and could be limited due to limited bandwidth of a RS-232 or RS-422 standards. The system offers

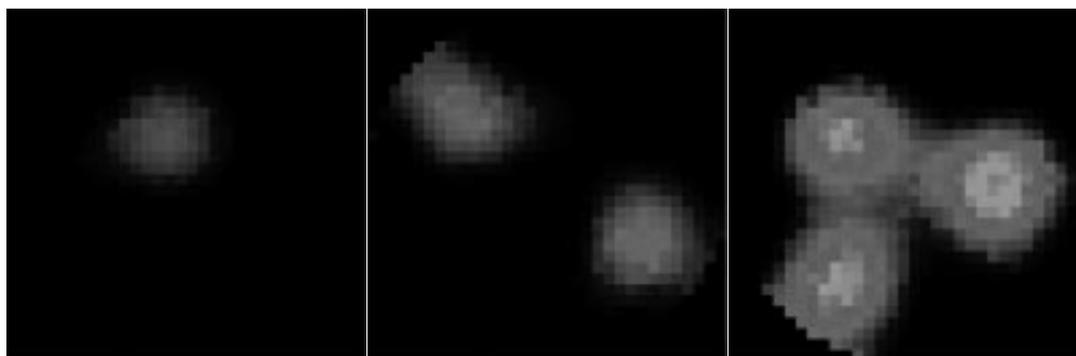


Fig. 4. First images from the ET2 tomograph: one, two, and three polypropylene rods.

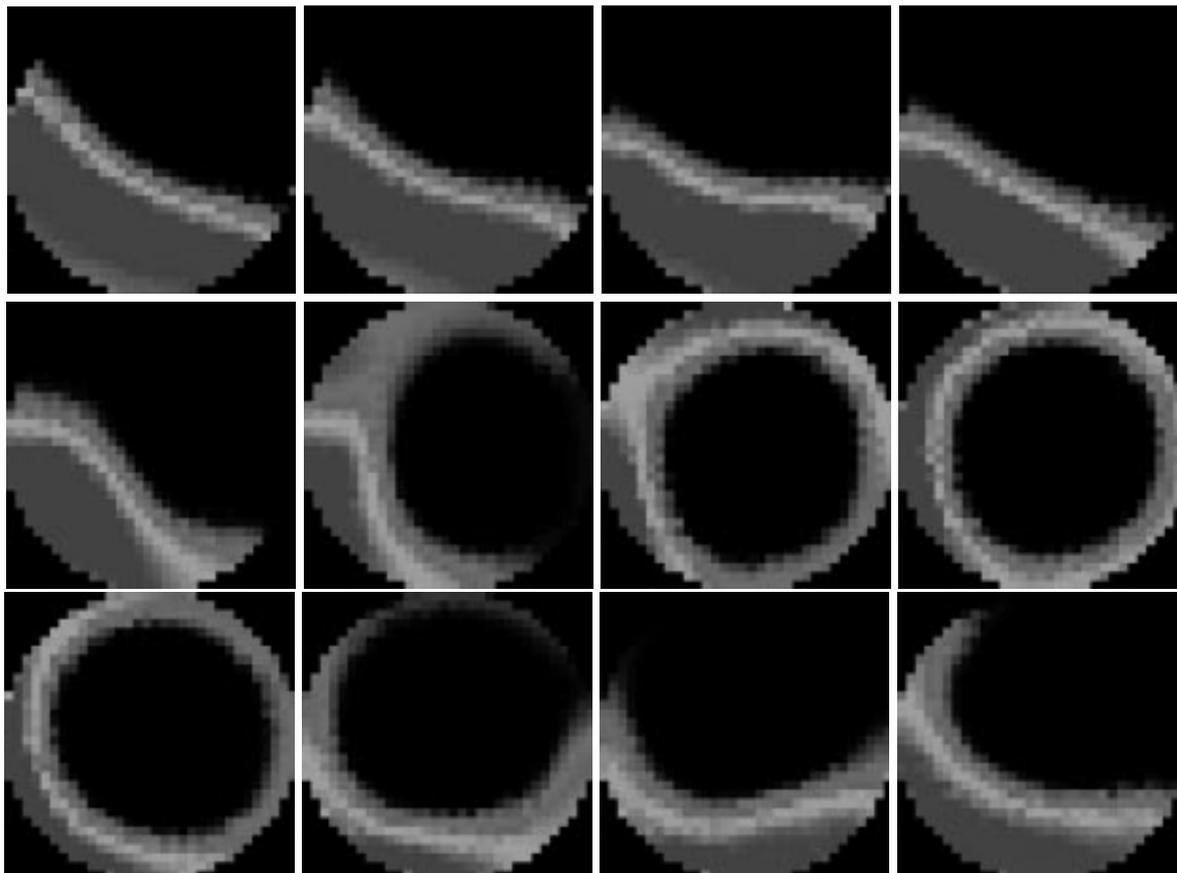


Fig. 5. The flow images of the oil in the shaken probe.

real-time image reconstruction. The image matrix is 32×32 pixels wide. The obtained images showed that the spatial resolution is acceptable and the real time presentation is possible.

The future work includes the following issues: optimisation of a capacitance measuring circuit to achieve smaller signal fluctuation, application of a controlled amplification to increase signal to noise ratio for the opposite electrodes and iterative algorithms for image reconstruction to improve image quality.

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