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Video-rate multiplexed driving scheme for passive antiferroelectric liquid crystal displays

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Antiferroelectric liquid crystals have been applied to high-end multiplexed displays. The interest on these materials chiefly comes up from their capability of being multiplex addressed with no need of active matrices. Antiferroelectric grey levels arise from a double symmetric hysteresis loop that can be stabilized by a constant holding voltage. Driving schemes are compatible with passive multiplexing, but limitations appear when the multiplexing rate increases. To avoid these limitations, new driving schemes for high multiplexing level at video rate have been designed. The problem of accumulated voltage on bias level arising from data voltages is tackled as well.

Keywords: antiferroelectric, liquid crystal, display, multiplexing, waveform, video-rate.

1. Introduction

The use of antiferroelectric liquid crystals (AFLC) as high-end displays (i.e., video rate, analogue grey scale, high resolution displays) was proposed ten years ago, soon after these materials became available [1,2]. This first attempt to take advantage of their fast response and multistable behaviour [3], nevertheless, was precluded by a number of difficulties, the most demanding being the lack of suitable materials and the reduced contrast of the display upon passive multiplexing, derived from the so-called pretransitional effect [4]. At present, the origin of pretransitional effect seems to be well understood [5], and the contrast problem has been substantially overcome with the advent of orthoconic materials [6]. It is therefore convenient to reevaluate the possibility of AFLC passive multiplexing in high resolution displays.

Driving schemes for these displays are applied on passive matrices arranged in rows and columns. Rows are sequentially selected while data are simultaneously applied to all columns. The schemes are based on short selection pulses and a common bias voltage that holds the grey levels induced on every pixel employing a combination of row selection pulses and column data pulses. It is important to realize that bias voltage is the same for any desired grey level (Fig. 1). Therefore, bias can be included as a component of the row addressing signal (applied along most of the frametime, in fact), and passive multiplexing can be employed. Should the holding voltage be different for every grey level, as in nematics or V-shape smectic materials, the use of active matrices becomes mandatory, as different voltages would have to be simultaneously applied to different pixels.

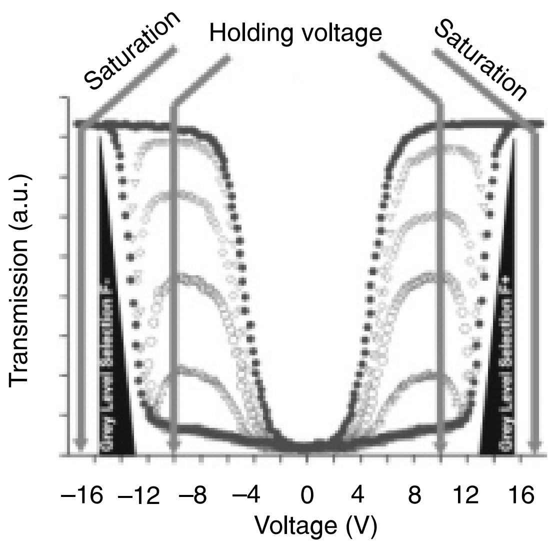

Fig. 1. Low frequency triangular waveform electro-optic AFLC response. Grey level selection is performed on the outer slopes of the hysteresis cycle. When voltage is reduced, different grey levels are shown and held by a constant voltage.

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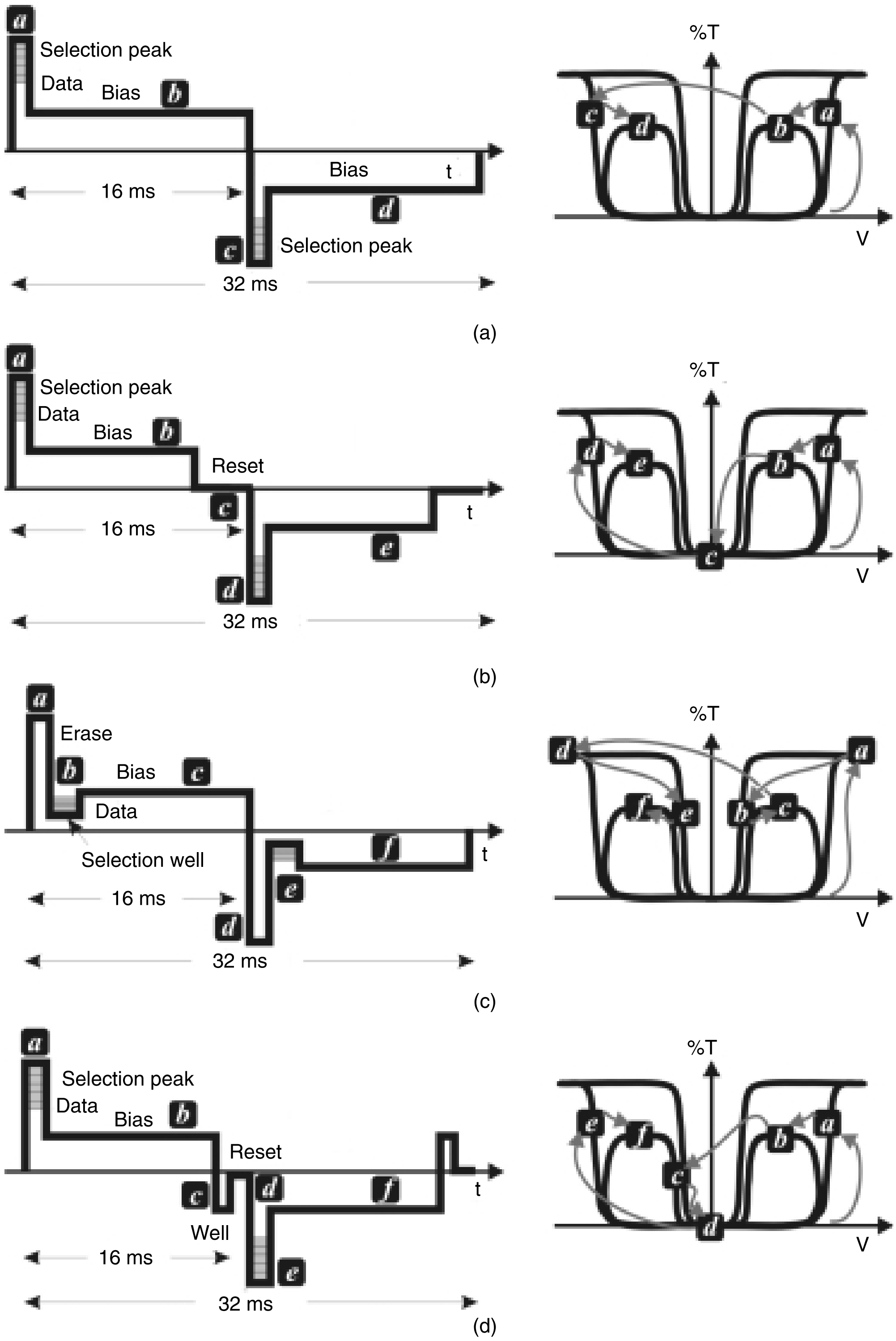


Fig. 2. Classic waveforms used to address multiplexed passive displays. (a) Basic waveform for AFLC driving, (b) same as (a) including a relaxation (reset) step, (c) Waveform based on interframe pixel blanking by saturation, (d) Waveform with forced relaxation to shorten reset time. Data are included onto the selection pulse in (a), (b), and (d). A data well is used in (c).

The basic waveform for AFLC passive multiplexing is shown in Fig. 2(a). It substantially consists of a selection pulse applied to a row followed by a holding voltage or bias voltage that covers the remaining fraction of frametime (more than 99% typically). During the selection pulse all data corresponding to its row are applied in parallel. A subsequent negative cycle is used to balance the positive and negative branches (DC compensation) avoiding pile-up of charges onto the electrodes.

In any passive multiplexed driving scheme, for a constant frame rate, the higher the resolution of the display, the shorter the slot time available for each row. As a consequence, the row selection voltage must be increased. This effectively reduces the multiplexing capability of antiferroelectric displays, ultimately setting the actual limit for row resolution at a given frame rate. The limit for current AFLC materials is about 30–40 µs; using these slots for selection pulses, a video-rate display working at 60 Hz (16.6 ms frame duration), could multiplex about 550 lines (1100 using dual scan). Selection pulses and data voltages for these tiny slots are rather high. Typical selection voltages at a room temperature are about ± 40 V while the data pulses about 8 V are needed to develop the whole greyscale.

If the target is a colour display, then the number of pixels is three times as much, increasing the number of rows and/or columns. As a consequence, manufacturing passive high-resolution video-rate colour displays becomes a challenging task. At present, the problem is customarily overcome by using active matrices and ad-hoc waveforms [7].

In this work, we present a new driving scheme that results in a 40% faster switching time. This time reduction can be directly employed to reduce the minimum slot time; alternatively, the selection pulse amplitude and data voltage range can be reduced.

2. Experimental

2.1. "Classical" waveforms for passive matrix displays

Some waveforms tested in AFLC passive driving are shown in Fig. 2. An outline of each waveform is presented on the left part, and the corresponding evolution of the voltage pulses on the hysteresis cycle is sketched on the right. The evolution picture is just qualitative, voltage amplitudes of the different waveform sections obviously depend on the actual frame rate.

The simple selection bias scheme mentioned above [Fig. 2(a)] cannot be used in practice, since AFLC materials show some kind of memory by which the grey level achieved during one cycle for a specific data voltage depends on the grey level of the previous cycle. This undesirable dependence must be avoided to achieve reproducible greyscales. It becomes necessary to include a blanking or erasing step in the basic waveform in order to bring pixels to a known state (always the same) before every cycle. There are three known states in AFLC hysteresis loops: the relaxed AFLC state at 0 V and the two symmetric saturated FLC states at the outer ends of the loops [8]. This opens up two driving possibilities depending on whether the starting point is one of the symmetric ferroelectric states [9] or the antiferroelectric state. Figure 2(b) shows a waveform based on relaxation. Greyscales achieved by this driving scheme are usually stable and almost linear, however, the reset time extends typically over several ms, making the waveform impractical for high refreshing rates, e.g. video. The driving scheme shown in Fig. 2(c) [10] is an alternative based on FLC saturation rather than relaxation (i.e., the AFLC state at 0 volts is never reached). The greyscale is developed through a "data well" right after the saturation peak. This strategy yields faster driving schemes, but greyscales are less satisfactory. Moreover, it is necessary to switch off the display backlight during saturation; otherwise interframe transmission maxima would reduce dramatically the display contrast. Finally, Fig. 2(d) shows a waveform proposed by our group [11]. It is based on relaxation, the slow relaxation process is sped up by a previous counter pulse (well). The scheme can be used with existing materials at a video rate, with some limitations commented below. It must be stressed, however, that this driving scheme may require two extra voltage levels (total, 7 levels).

2.2. Increasing multiplexing level

Whatever the waveform, it is sequentially applied to the rows, shifted a temporal slot corresponding to the width of the selection pulse (Fig. 3). As mentioned above, if a video rate (e.g. 60 Hz) antiferroelectric display is to be designed, increasing the multiplexing rate reduces the switching pulse width and consequently the threshold voltage and data voltage range are dramatically increased. Figure 4 shows the evolution of the required voltages for 70, 50, and 30 µs selection pulse slot widths. These slot times correspond respectively to the displays having approximately 240, 330, and 550 rows, working at 60 Hz.

If the multiplexing increases a rate from 240 rows to 550 rows, the threshold voltage increases from 29.8 V to 38.4 V. Even worse, the dynamic data range increases from 5.8 V to 11.6 V. While the first issue can be solved

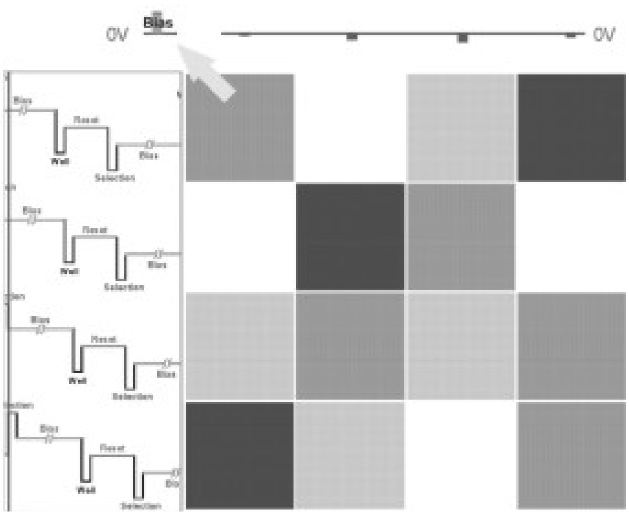
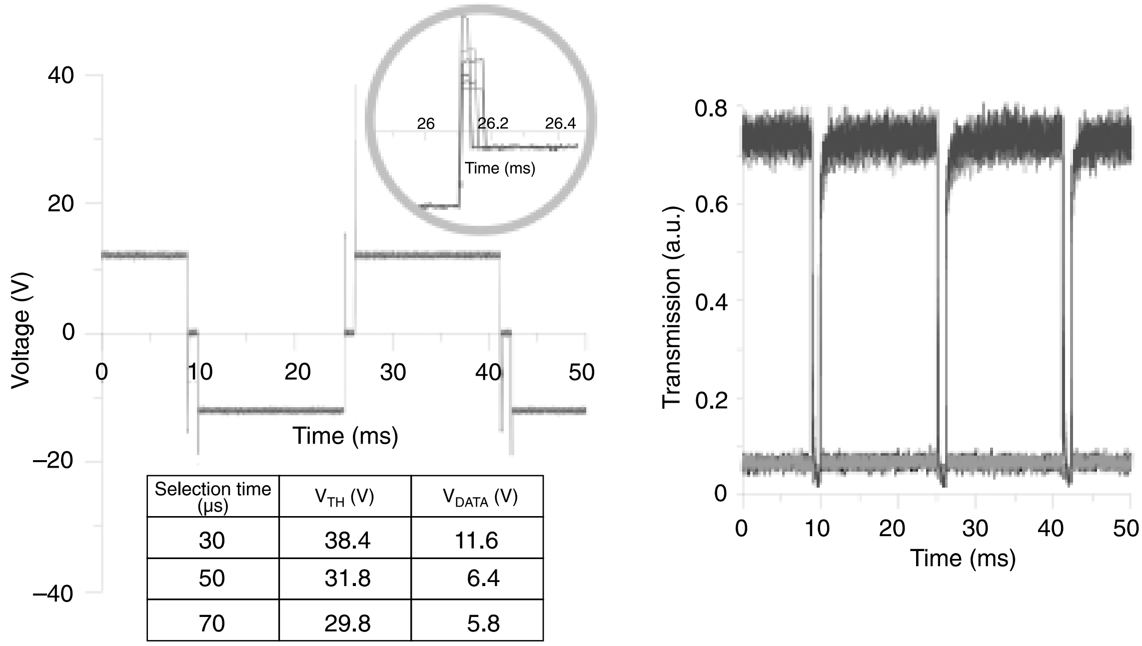


Fig. 3. Multiplexing scheme. Frametime is distributed in as many slots as the number of display rows. Rows are sequentially addressed, each row being delayed one slot from the previous row. The selection pulses extend over the whole row slot to minimize its amplitude.



Selection time (μs)	V_{TH} (V)	V_{DATA} (V)
30	38.4	11.6
50	31.8	6.4
70	29.8	5.8

Fig. 4. Variation in threshold voltage and dynamic data range upon reduction of slot time (see inset) corresponding to a video-rate SXGA monochrome display.

with existing electronics, the second unveils a problem often arisen in multiplexed AFLC materials driven in passive matrices. Indeed, a crucial condition for a passively multiplexed AFLC display to work correctly is that the ratio between the dynamic data range and the holding voltage (bias voltage) must be kept as low as possible. When the grey levels of any given display row are stabilized by a DC bias voltage, every pixel of the row "sees" the data voltages applied to the remaining display rows along the frametime while the rows are being selected. Data voltages, therefore, are added up to the bias voltage. The bias voltage level is customarily selected taking into account the average data voltage, in fact, on-line bias level corrections may be included in the waveform using buffers where data can be weighted in advance; but this solution does not guarantee a correct greyscale under all circumstances, because passive multiplexing demands the bias level to be the same over the whole display. Intermediate grey levels will drift to brighter levels if the remaining display area is bright, or to darker levels if the remaining display area is dark. Obviously, the effect is more noticeable as the ratio between data range and bias voltage increases. In the example of Fig. 4, the required bias voltage for grey level stabilization is about 12 V. Therefore, the voltage ratio is approximately 1:2 for 70-μs selection time while reduces down to 1:1 for 30-μs selection time; this ratio is not valid in practice.

2.3. Designing new waveforms

The existence of a memory effect upon switching, as described above, can be reinterpreted in the following way: if the same selection pulse produces different results on pixels previously having different grey levels, the dynamic response is modulated by the pixel transmission. Indeed, it can be experimentally shown that the addressing and data voltages required for obtaining any grey level decrease as long as the liquid crystal is far from equilibrium (i.e., far from AFLC state). Consequently, faster switching rates and/or lower switching voltages, could be obtained by including a prepulse (awakening pulse) in the waveform before the selection pulse. The scope of this pulse would be to bring the pixel out of the relaxed state, allowing the selection pulse to drive the pixel to its required transmission state in more favourable conditions.

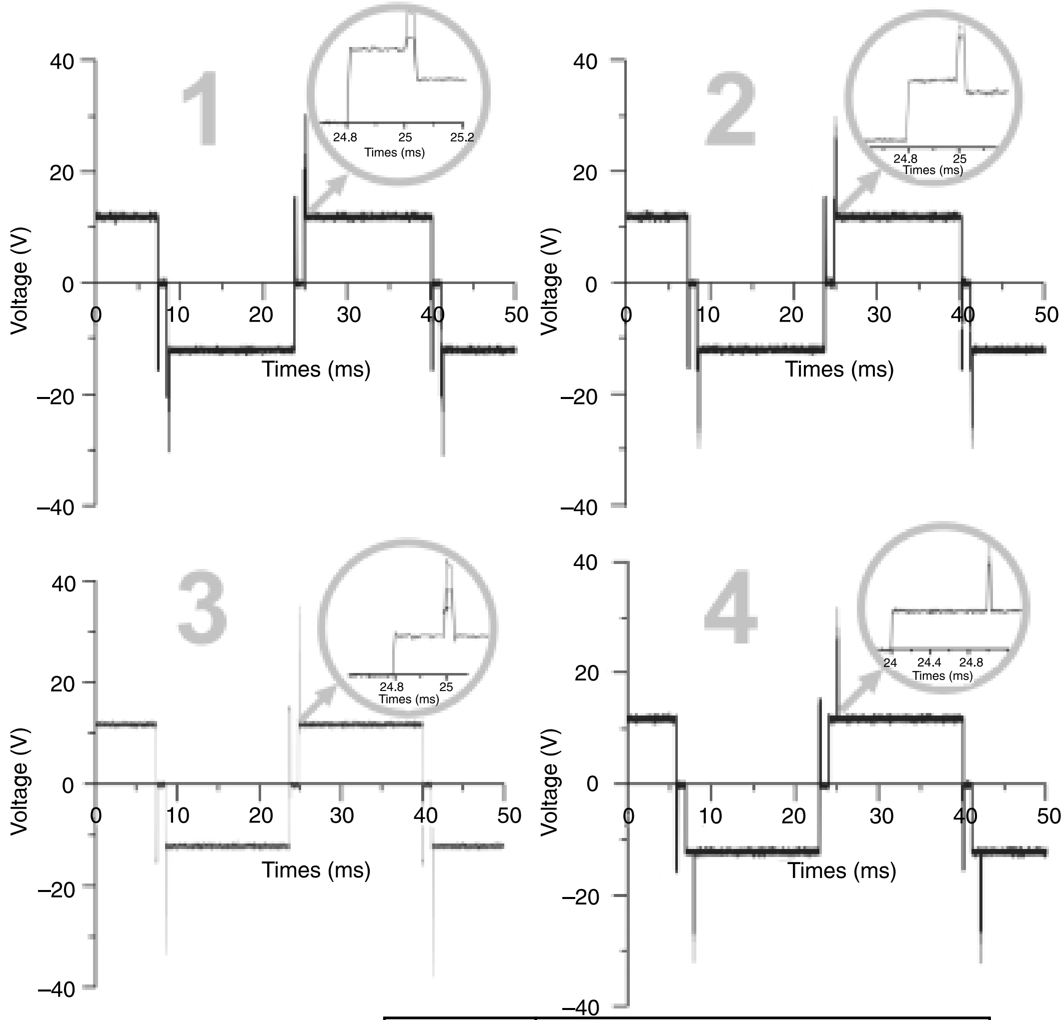
A second issue that should be improved is the correction of residual DC. In principle, DC is automatically compensated by the alternative utilization of the positive and negative branches of the hysteresis loop. However, the data introduce extra voltage levels that may or may not be compensated within the symmetric addressing waveform. Even in a homogeneous display, data voltages modify the bias level of the waveform. When data are not compensated, the intermediate grey levels are altered because of bias voltage fluctuations derived from data voltages of the remaining display rows. Although bias level has some tolerance, data above a certain limit shift the transmittance of other display rows. At present, the only proposed solution to avoid this crosstalk is to reduce the dynamic data range until the maximum data voltage is negligible as compared to bias voltage. Unfortunately, this is not the case in most video rate, high resolution AFLC systems, since they require reduced slot times customarily linked to wide dynamic ranges.

3. Results and discussion

3.1. Awakening pulses

We have explored four designs of awakening pulses for a display working a 60 Hz with 30 μs selection pulse. This slot is required to drive a video rate passive display of 550 lines (1100 using dual scan, i.e., enough for SXGA or WSXGA resolution):

- 200-μs awakening pulse, whose amplitude is high enough to partially switch the relaxed pixel. As it can be seen in the inset, this amplitude is significantly higher that the bias level.
- an awakening pulse of the same duration (200 μs) below the threshold voltage for this time width. In this case, the pulse amplitude is slightly higher than the bias level.
- 200-μs pulse of the same amplitude as bias (12 V in this example). This approach does not introduce extra voltage levels in the waveform, simplifying the driving electronics. The two previous designs increase the number of voltage levels of the waveform from 7 to 9.
- a longer awakening pulse (1 ms) maintaining the bias voltage. In this approach, the pulse length somewhat compensates the low voltage level of the pulse. Indeed, bias voltage is well below threshold, making it difficult for a short pulse to produce any noticeable effect.



	Clasic waveform	New waveform		
		2	3	4
V_{TH}	38.4	26	35.2	26
V (10% transmission)		26.4		26.4
V (90% transmission)		28.4		28.4
V (Saturation)	49.0	30.0	44.4	32
Data range (V)	11.6	4.0	9.2	6.0

Fig. 5. New proposed waveforms including awakening prepulses before the selection pulse. (1) 200-μs prepulse achieving partial pixel switching. (2) 200-μs prepulse below threshold level. (3) 200-μs prepulse at bias level. (4) 1-ms prepulse at a bias level.

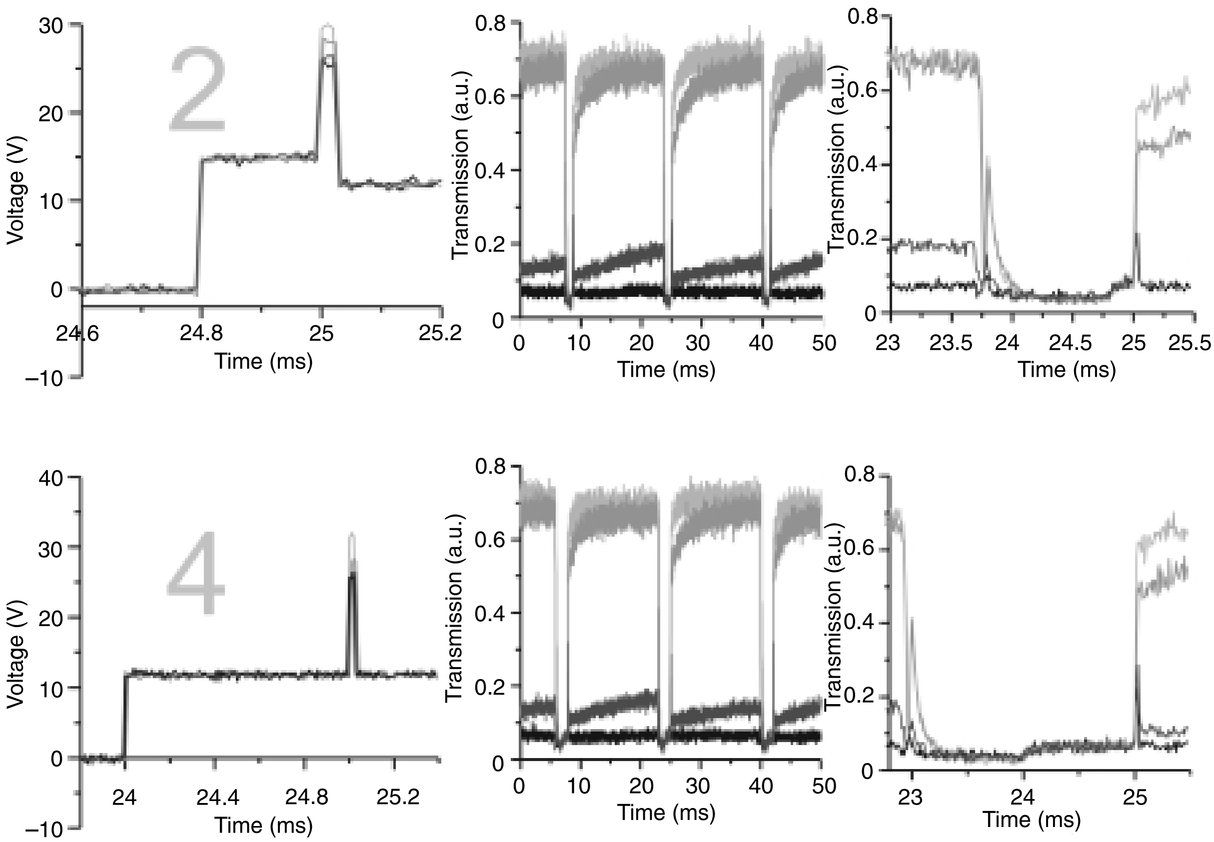


Fig. 6. Grey levels generated by two waveforms with awakening prepulse. A slight transmission increase is observed within the prepulse duration due to pretransitional effect.

The remaining sections of the driving waveform (i.e. bias voltage and duration, well voltage and duration and reset time) are kept constant.

Figure 5 summarizes the results. Waveform 1 shows non reproducible results, and is under study. The inconsistency of the results is attributed to the variable effect produced by the partial switch achieved by the awakening pulse, depending on the original pixel state. As expected, improvement in the response of the conventional waveform by the third waveform is negligible. The awakening pulse is too low in this case, and too short as well.

Best results are obtained with the second and fourth waveforms (Fig. 6). In both cases, the 30-µs response is slightly better than the 70-µs response of the classic waveform, as shown by their threshold voltage and data range. This should be considered a relevant improvement in the dynamic response. Comparing dynamics of cases 2 and 4 in our example, it is found that threshold voltage and 10–90% dynamic range voltages are the same, however, saturation in case 2 is two volts lower than in case 4. As lower dynamic ranges are preferable, waveform 2 should be considered in principle superior to waveform 4, for its dynamic range is narrower. Nevertheless, both waveforms can be used between threshold and 90% transmission with an excellent data range (2.4 V) giving a decisive advantage over former classical waveforms. On the other hand, electronic implementation of waveform 4 is more straightforward since no extra voltage levels are required (waveform 2 requires up to 9 voltage levels). The best solution shall be a tradeoff between electronic complexity and electrooptical performance.

3.2. Avoiding crosstalk

Although the new proposed waveforms show remarkable advantages over the previous 7-level waveform, the problem of uncompensated data voltages remains unsolved. The example shown in Fig. 7 corresponds to two extreme cases. A grey line with 50% transmission is drawn on an otherwise white or black display. The response of waveform 4 adjusted to the intermediate grey level shows severe deviations of the expected transmission towards lighter or darker greys, respectively. Deviations are produced by the "noise" arising from data pulses, because the bias level is shifted up and down over the dynamic data range.

An elegant solution to this problem is proposed (Fig. 8), making use of the fact that contiguous rows usually hold the same or very similar grey level data. The waveform applied to odd rows is shifted half a period, so that alternative positive and negative addressing pulses are used. The corresponding data pulses shall be made positive and negative correspondingly. Therefore, data voltage levels are cancelled out on every pair of rows, assuming their data grey levels are the same. As a consequence, most data voltages av-

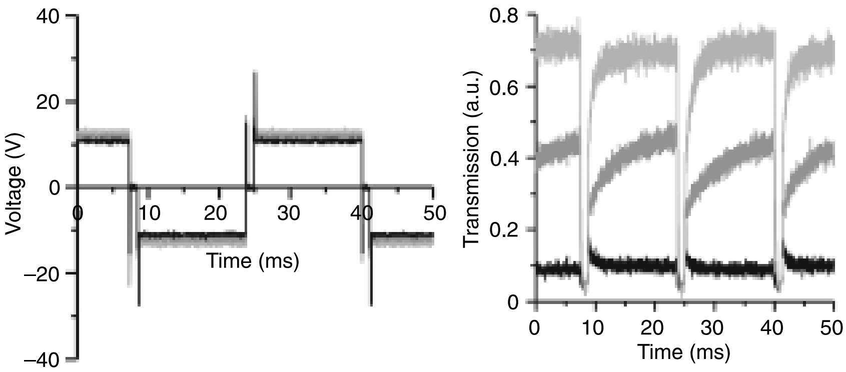


Fig. 7. Three responses obtained for the same intermediate grey level data. Bias levels are modified by the presence of data from other rows. The whole dynamic range has been taken.

erage to zero, the residual DC being easily tolerated by the grey level hysteresis plateau.

4. Conclusions

The new waveforms proposed in this work show an excellent dynamic behaviour under high multiplexing rate allowing the design of passive high resolution displays at a standard video rate. Two waveform modes improving multiplexing rate have been described. In one of them, the number of voltage levels of the addressing waveform need not be increased; therefore the same driving electronics can be used. A simple solution to the problem of bias voltage oscillations depending on data values has been presented, using alternating scanning of odd and even rows. These experiments demonstrate the possibility of driving passive SXGA antiferroelectric displays with an analogue greyscale.

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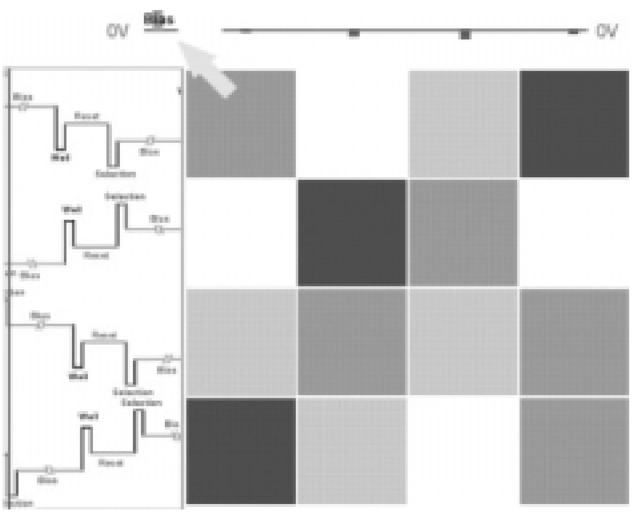

Fig. 8. Alternating scanning provides a straightforward solution to avoid the effect of uncompensated voltage data on bias level.

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