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Overview of etching technologies used for HgCdTe

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This review is an attempt to survey all the etching techniques that have been used since the very beginning stages of HgCdTe device fabrication to the most recent ones. Recent state of the art device architectures such as high-density focal plane arrays, avalanche photodiodes, two-colour and multispectral detectors require isolation of high aspect ratio trenches with least etch induced damage at the surface and sidewalls. The most widely used dry etching techniques are electron cyclotron resonance plasma and inductively coupled plasma processing. Almost all the etching technologies have been summarized from chemistry and device perspective.

Keywords: wet and dry etching, mesa etching, ECR plasma system and etch lag.

1. Introduction

Fabrication of HgCdTe devices has always been a challenging task for process engineers due to sensitive nature of the material. The alloy has lower damage threshold and greater defect density in comparison to wide gap semiconductors (Si, GaAS, GaN etc.). Therefore, extensive care has to be taken during each and every process step involved in fabrication of mercury cadmium telluride (MCT) devices. One of the very critical process steps, involved in the sequence of fabrication processes, is etching of the compound semiconductor, wherein images have to be transferred irreversibly into the wafer.

The device technologies based on MCT have advanced considerably over the last few years. A large chunk of the market for HgCdTe devices is based on photoconductive or photovoltaic (scanning or staring) mode of detection. I-generation arrays had 60, 120, and 180 elements in scanning configuration. They were replaced by II-generation 240×4 and 480×4 scanning array photodiodes; staring mode focal plane array pixel count has risen from 256×256 to 2052×2052 in 2000 [1], it is still expected to rise to 10k×10k by the year 2010. Although the Moor's law for Si semiconductor industry holds good for MCT based devices, but the trend followed is increase in the number of pixel counts in the scanning or staring arrays over time, shrinkage of critical device dimensions has not been as dramatic as for Si memory chips. Recently nanometer scale structures such as quantum wires, quantum dots, medium wave and long wave infrared lasers and infrared nonlinear optical switches have been fabricated [1–3]. Fabrication of such devices requires transfer of high aspect ratio patterns with good anisotropy and least structural and electrical damage. Etching of HgCdTe is a complex process and the etch parameters are not always predictable. Etch performance is determined in terms of etch rate, selectivity, uniformity in a batch and across the wafer, reproducibility, micro loading effects, surface roughness and device damage, critical dimension and profile control. Features with high degree of anisotropy can be defined using dry etching techniques. An in-depth understanding of etching mechanisms requires knowledge of diverse fields of chemistry, physics, and electrical sciences. To have a good control, the etch process needs to be optimized for reproducibility and uniformity over large areas of a device. Thus, it becomes necessary to generate a lot of data related to the parameters involved in the etching process. Kinetic variables such as activation energy, viscosity (flow dynamics in gas phase etching), etch rate, composition of etchant and surface effects such as type conversion, lattice damages etc. need to be determined through experimentation.

2. HgCdTe etching technologies

Etching is an integral part of HgCdTe infrared detector processing sequence. Figure 1 shows the different wet and dry chemical techniques that have been developed since the very beginning stages of HgCdTe device fabrication to the most recent ones. I-generation linear detector arrays require patterning of feature sizes 50–60 μm wide, that can be successfully done using traditional wet chemical etching. Wet etching techniques have been used since early phases of growth of the material, but only a few etchants have been tried. Widely reported wet etchants are that of alcoholic solutions of Br_2 (Br_2/Methanol, Br_2/HBr etc.) [4,5]. Wet etching is isotropic and the uniformity process is low. Production industries require more controlled etching performance than can be achieved using wet etching. II-generation two-dimensional arrays of photodiodes, high performance infrared focal plane arrays and superlattice structures re-

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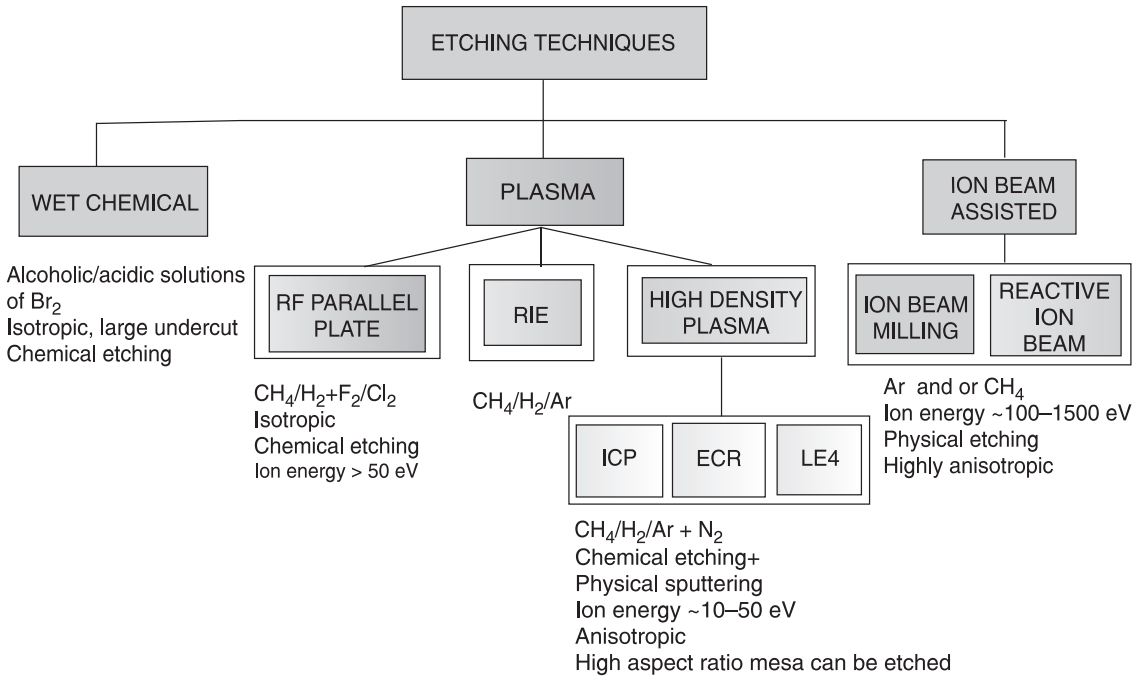

Fig. 1. Different dry etching techniques that have been used since the beginning of HgCdTe device fabrication. Traditional wet etchants are alcoholic/acidic solutions of Br_2. Dry etching techniques utilize various combinations of CH_4, H_2, Ar and/or N_2 plasma.

quire mesa isolation of diode pixels. The requirement of deep, narrow sloped trenches with high aspect ratios, smooth sides and high uniformity, gave impetus to development of dry etching. Plasma etching in methyl afterglow reactor using Cl_2, CH_4 and H_2 [6], atomic F [7], RIE with CH_4 and H_2 [8], H_2/Ar magnetically enhanced ECR plasma [9] and ECR RIE [10,11] were developed as a consequence. III-generation devices such as two-colour detectors, APD's and hyper spectral arrays that are in developmental phase today require deep isolation trenches with high aspect ratios (15 μm deep trench with 20 μm pitch [12]), likewise the APD's need etching of via holes with minimal surface damage. Nanostructures require high resolution patterning of MCT with high degree of anisotropy and least damage. These structures need highly advanced high-density plasma (HDP) reactors for the purpose.

3. Wet chemical etching

The Internet search for data on wet chemical etching of HgCdTe revealed very little amount of information on the variety of etchants used. Traditional etchants for MCT are Br_2 based chemistries. Typically alcoholic solutions of Br_2 (Br_2/Methanol, Br_2/Butanol, Br_2/Ethylene glycol or a mixture of these in various concentrations) have been used for CdTe or HgCdTe etching [4,13,14]. Wet chemical etching proceeds by oxidation of the semiconductor constituents (HgTe, CdTe) followed by chemical dissolution of the oxides in suitable solvents. An investigation of etching of mesa structures in Br_2/HBr/ethylene glycol showed reproducible vertical and lateral etching with smooth (rms roughness of ~2–3 nm) damage free surfaces and sidewalls [14]. Wet etching is advantageous over dry etching because of least structural and electrical damages to the wafer. Most of the data published on wet etching of HgCdTe report the results of surface analysis using photoluminescence spectroscopy [15,16], X-ray photoelectron spectroscopy [4,13, 16], Rutherford back scattering [17], Auger electron spectroscopy [18,19] etc. based on the analysis, one can infer that the etch rate of Cd > Hg > Te, for the composition ratio remaining on the surface is Hg: Cd: Te: 0.4:0.08:1, for all concentrations of Br_2 (0.05% to 10%) in different solvents [13]. All of the etchants leave the MCT surface Te rich. The greater etch rate of CdTe sub lattice in HgCdTe is confirmed by the study photo etching of $Hg_{0.1}Cd_{0.9}Te$ in strongly acidic solutions of perchloric acid (pH = 0; 0.35 mA/cm^2)[18]. Likewise electrochemical etching of $Hg_{08}Cd_{02}Te$ [20] in acidic solutions (pH = 4.9) under small reverse bias etches CdTe super lattice separately. Reagents used for Si or GaAs (Cl_2, Br_2, $Cr_2O_7^-$, H_2O_2, HNO_3, $HClO_4$ etc.) can easily oxidize HgCdTe provided the thermodynamic requirement $\Delta F = -nf\Delta E$ is satisfied, where ΔF is the change in free energy, ΔE is the difference between cathode and anode potentials and f is the Faraday's constant [21]. The free energy data for photo electrochemical etching of HgCdTe in various acidic and neutral solutions were calculated extensively by Tenne *et al.* [18]. The ΔF= 3.5 kCal/mol for CdTe and ΔF = 46 kCal/mol for HgTe. The inference is that the CdTe component is more amenable to oxidative reactions than the HgTe sublattice, although the Hg-Te bond is weaker than Cd-Te bond.

Larger ionicity of Cd-Te lattice favours greater hydration of Cd cations than that of Hg cations. At higher pH's (> 4) the tendency of formation of oxides of various

Table 1. Summary of wet etching processes for HgCdTe.

Etchant	Surface condition	Etch rate	Ref.
Br_2/Me (1–10%)	Te rich surface Oxides of Te possible Carbon contamination	~1 μm/min 7.3×([Br] in vol%)	17
Br_2/HBr (1–5%)	Te rich surface	As high as ~10 μm/min	–
Br_2/HBr/Ethylene glycol (in various ratios)	Oxides and carbon content. Almost stoichiometric	0.6–4 μm/min depending on composition of mixture	–
$K_2Cr_2O_7$:HNO_3:H_2O: 4 gm: 10 ml: 20 ml	Te and Cr oxides Carbon contamination	Used for selective etching of CdTe	22
Photo electrochemical etching in 1M $HClO_4$	Cd depletion, no oxides Mostly HgTe	Not reported	21
Photo electrochemical etching in 1M KCl	Te oxides Cd depletion	Not reported	21

cations increase and the surface chemistry is predominated by tellurium oxides viz. TeO_2, $CdTeO_3$, $HgTeO_3$ and CdO etc. because their solubility of Te and it's oxides is low in this range (pH = 7, neutral). In Br_2 solutions, the Br_2 molecules present in the solution are adsorbed on the crystal surface and react with Te^{2-} anions to leave Br^- anions and Te^0. The Br^- anions oxidize the Cd and Hg cations leading to formation of soluble Cd and Hg bromides (Br/HBr), in addition dimethyl Cd and dimethyl Hg are also probable volatile species (Br/Methanol/Butanol/Ethylene glycol). The thermodynamic probability of formation of Te^{4+} (ΔF = 55.8 kCal/mol for CdTe and ΔF = 98.5 kCal/mol for HgTe) is low because of large free energy barrier. The neutral Te^0 are removed in the form of atoms. Because of heterophase nature of etching of HgCdTe in acidic solutions, the surface uniformity and stoichiometry get altered. Te rich layer can lead to increased surface leakage across the p-n junction and degrade diode characteristics. The Te rich layer can be controlled by quenching the etch by methanol (mirror like finish). The Te rich layer, Te oxides and HgTe rich layers all can be removed by prolonged soaking in 10% KCN solution, thus retain surface stoichiometry [17].

Different wet chemical etchants of MCT and their effect on surface condition are reported in Table 1. The task of a process chemist is to first choose a suitable oxidizing (acidic/neutral) solution to etch the material of a given x value and then have a tight control over the process conditions. Three major process variations are thickness of the film to be etched, control of temperature, and time to the end point. Agitation of the solution can be a parameter for diffusion controlled reactions, but generally wet etching is a rate-controlled reaction [14]. Wet etching is these days limited to only surface preparation of HgCdTe, it is difficult to control because of non-uniform etch rates and isotropic nature of process needs high etch bias.

4. Dry etching

Development of dry etching processes for II-VI semiconductors started by late 1980's and early 1990's. It was soon realized that relatively low energy ion bombardment (~100 eV or less) is required for the sensitive etching process to reduce ion-induced damage. Development of various etching techniques for the material has essentially followed and gained from the sequence of dry processing technologies that have been used for fabrication of group IV and III-V compound semiconductor devices. Most of the III-V's (GaAs, InP, GaP, GaN, InAs, InSb) and group IV elemental semiconductors have been processed using halogen (F_2, Cl_2, Br_2, I_2) based plasma. The chemistry of volatilization of HgCdTe is difficult to understand and control as well, since the etchant has to remove three constituents simultaneously. Very initial attempts towards dry etching of II-VI compounds were based on halogen (Cl_2, F_2) based glow discharges [7,22], but Cl_2, F_2 etching chemistries are not viable for HgCdTe due to low vapour pressure of Cd halides [23]. In addition, these reactants and products proved to be corrosive and toxic. Later on CH_4/H_2 and CH_4/H_2/Ar based chemistries were favoured for plasma etching of the semiconductor [23–25]. In fact, the hydrocarbon/H_2 based methyl radical etching chemistry has been used extensively, albeit the kind of plasma reactor design has varied from RF glow discharge, reactive ion etching (RIE), magnetically enhanced RIE (MRIE) configuration, low energy electron enhanced etching (LE_4) to the electron cyclotron resonance (ECR) system. All these plasmas are called low pressure (10^{-4} to 10 Torr) or cold plasma, wherein the density of charged ions and radicals is relatively smaller than that of the neutrals; the energy of ions and radicals involved in etching process is low (10–50 eV) and hence are suitable for patterning II-VI alloys with minimal damage. Ion beam based dry methods include reactive ion beam etching (RIBE), chemically assisted ion beam etching (CAIBE) and ion beam assisted etching (IBAE). These processes are associated with relatively high ion energies (100–1000 eV), but are highly anisotropic and can be used for etching fine features in HgCdTe (Fig. 1). As most of the practical aspects of material and devices have been discussed we will straight away go into details of different dry etching methods used till date.

4.1. Plasma etching

The fundamental requirement of dry plasma etching is that the reaction must be exothermic and the reaction products should be volatile. Halogen based dry etchants do not produce volatile products for at least one of the elements in CdTe, HgCdTe and InSb at reasonable temperatures. The fact that HgCdTe can be grown by metallorganic chemical vapour deposition (MOCVD) using dimethyl cadmium, dimethyl tellurium and Hg vapours as sources, lead to different etch strategy using formation of volatile organo-metallic species as etch products [2,5]. Purely chemical methyl free radical etching of HgCdTe, CdTe, and InSb in a secondary after glow reactor using $CH_4/H_2/F_2$ is reported by Spencer *et al*. [26,27]. Figure 2 shows the afterglow reactor used in the process, the 2.45 GHz microwave discharge is located upstream of the workpiece. The products of the discharge passing out in the afterglow are dissociated atoms (generally O, F, or Cl) that have longer lifetimes termed as primary afterglow discharge. The primary discharge species react with stable species in the afterglow (CH_4, H_2) to produce highly reactive polyatomic free radical species termed as secondary afterglow, these are used for wafer processing. Atomic fluorine that assists formation of CH_3 and atomic hydrogen is produced in a pressure stabilized 2.45 GHz microwave discharge of SF_6 and Ar. Fluorine afterglow is then introduced into the stainless steel main chamber where H_2 and CH_4 are mixed in a

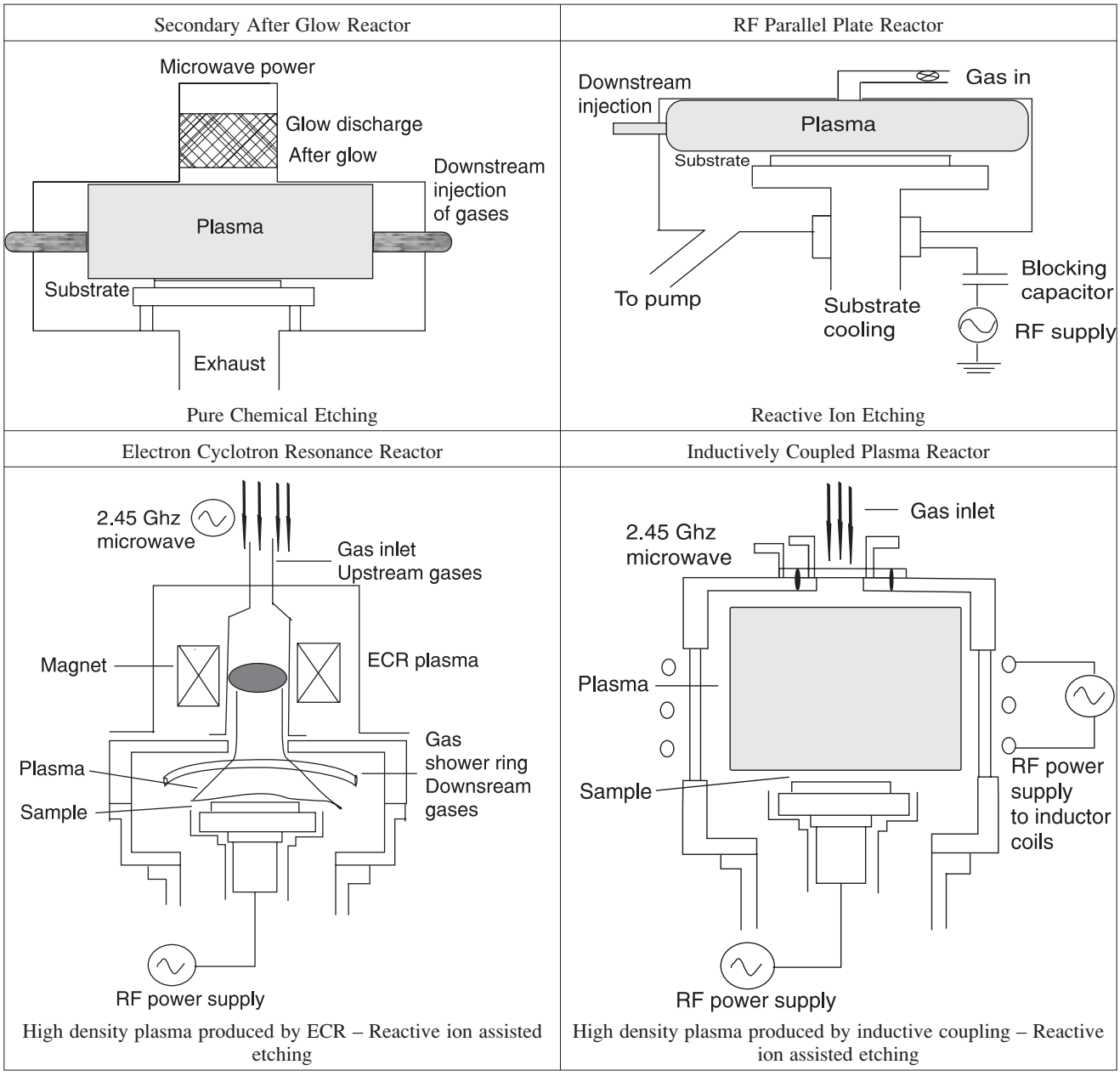

Fig. 2. Schematic of different kinds of reactors used for etching HgCdTe.

5:1 ratio and diluted in Ar, these are the stable secondary reactants. The plasma reactions responsible for etching of the semiconductors are

$$F + CH_4 \rightarrow CH_3 + HF,$$
$$F + 2H \rightarrow H + HF.$$

Methyl radicals and hydrogen atoms generated by downstream reactions of atomic fluorine, methane and hydrogen are quite reactive towards CdTe, HgCdTe. But the HgCdTe surface etched in the reactor is quite rough and damaged as compared to CdTe because of its weaker crystalline nature. The mechanical damage is not merely confined to surface but penetrates deep into the bulk. The etch process is purely chemical and etch profiles are isotropic. The applications of plasma etching nowadays are mostly limited to cleaning surfaces or removing unwanted materials such as layers of photoresist, polysilicon or SiN_3 that have served their purpose and are no longer needed.

4.2. Reactive ion etching

Reactive ion etching (RIE) is defined as plasma etching, where pattern transfer is accomplished by a combination of chemical activity of reactive species and physical sputtering by energetic ions (> 50 eV). The application of RIE to microelectronic fabrication of high-density integrated circuits was made possible through several pioneering studies in the mid 1970's [28–30]. These studies revealed that in certain gas – solid systems in which volatile etch products are formed; a simultaneous positive ion bombardment greatly increased the etch rate. Furthermore, because of directional ion bombardment along with reactive ions highly anisotropic etching of small features could be established [31]. It is well known that physical sputtering is unsatisfactory for high aspect ratio pattern transfer in HgCdTe. RIE and hybrid electron cyclotron resonance-RIE of HgCdTe and other II-VI semiconductors use H_2 or CH_4/H_2 mixtures in a parallel plate, single radio frequency power supply configuration (Fig. 2) that can sustain plasma density of ~10^9 cm^{-3}. The gaseous species from the plasma interact with the surface atoms forming volatile species and can produce mesas with dimensions in the range of 2–40 μm [32–36].

RIE has been used as a means for providing mesa isolation of epilayers of both photoconductive and photovoltaic device structures [37]. Table 2 lists the process details of RIE of HgCdTe followed by different workers and the salient features of their analysis. From the data and analysis it

Table 2. Process details for RIE of HgCdTe in RF parallel plate reactor.

Reference	31	32	32	35	36
Device/feature	Interdigitated structure, width of 2.3 μm, spacing of 3.3 μm	Via etch	Via etch	–	Mesa isolation of PC and PV devices
X, type of material	0.2, 0.8, MOCVD	0.22, SSR, LPE and THM	-Do-	1, LPE epilayers (100) oriented	0.31, LPE, p-, n-type HgCdTe
Operating pressure (mTorr)	20	60	60	64	40
H_2 flow rate (sccm)	–	1150	1150	30	–
CH_4 flow rate (sccm)	85 (total flow)	–	300	3	30 (total flow) CH_4:H_2: 1:5
Substrate temp. (°C)	35	5	5	–	16
Rf power	150 W	0.62 mW/cm^2	0.62 mW/cm^2	300 W	0.4 mW/cm^2
DC bias(volt)	–360 to –440	80	70	–	180
Analysis techniques	Laser interferomtry, RBS, SEM	XPS, ICP analysis, OES, SEM	-Do-	SEM	LBIC, SEM
Surface roughness	Sidewalls rough	Very rough ~300 nm	Reduced roughness	Quite rough	Rough
Remarks	Roughness is due to high rf power induced DC bias	White coloured fluffy residue of a Cd enriched layer is responsible for roughness removed by a dip in 10% HNO_3, Via A.R. ~0.5	Via A.R. improved to 0.9, and etch rate increased. This is correlated to reduced surface roughness	Anisotropic etch figures delineated. Polymer deposition observed for CH_4 fraction >10%	Type conversion of n to n+ and p to n around the etched surface

is evident that parallel plate RIE using CH_4/H_2 plasma can transfer fine features into HgCdTe with high degree of anisotropy. Primary reaction products in the discharge determined from mass spectrometry measurements are elemental Hg, TeH_2, $Hg(CH_3)_2$ and $Cd(CH_3)_2$, confirming the fact that hydrocarbon etching of the material is a reverse MOVPE process and termed as metal organic reactive ion etching (MORIE) [32,36]. However, there are certain aspects to be considered:

- the process results in rough surfaces, roughness can be as high as ~200 nm. This roughness is attributed to a multitude of factors, such as preferential etching of HgTe which leaves behind a Cd rich surface, polymer deposition when CH_4 fraction in the plasma is high and high rf power induced DC bias that results in high ion energies and thus ion induced damage,
- since the process is ion assisted, physical and electrical damages to the semiconductor may occur such as p- to n-type conversion and alteration of near surface stoichiometry,
- when CH_4/H_2 ratio is less than 1:3, the probability of formation of polymer film increases [37] that could act as etch stop mechanism.

Type conversion, changes in stoichiometric composition, surface roughening and polymer deposition can be controlled in RIE process by optimizing the process parameters such as CH_4/H_2 ratio, total pressure, temperature and incident ion energies. In fact, the desirability of RIE for etching and structuring of HgCdTe has been rather limited because of these effects. It has rather been used for p- to n-type conversion and inducing stoichiomeric variations for fabricating photodiodes and other novel device applications [38–40].

Reduction of ion-induced damage is very critical for etching HgCdTe devices. The etch rate depends on ion power density incident on the wafer, hence as ion energy is decreased it becomes necessary to increase the ion flux to maintain reasonable etch rate. The plasma density available by 13.56 MHz RF capacitively coupled plasma is limited ($< 10^9$–10^{10} electrons/cm^3, current density < 1 mA/cm^2) by the power dissipated in the electrode due the high-energy ion bombardment and by the accompanying sputter erosion of the electrode.

A solution of this dilemma is the use of a high-density plasma system. In high-density plasma systems, independent control of ion energy and ion flux is obtained. Typically, the power used in high-density source (source power) is much higher than the bias power (power applied to the wafer bearing electrode). Hence, the bias power does not contribute significantly to the plasma density and the ion flux is essentially independent of the bias power. It is well known that bias power is approximately equal to the product of ion energy and ion current. Therefore, if ion current is increased by increasing the source power (keeping bias power constant), the ion energy must decrease [41]. This principle is used for the design of HDP reactors such as ECR and ICP systems.

4.3. Electron cyclotron resonance etching (HDPE)

Anisotropic etching is achieved by unidirectional ions produced when ion mean free path is larger than the width of cathode dark space. These conditions are produced in RF parallel plate reactor by reducing pressure and producing large sheath electric fields, which are required for effective RF coupling to the plasma. This situation, in which energetic conditions at the substrate are tied to maintenance of plasma, results in unfortunate characteristic that as the pressure is reduced, the substrate bias becomes large (several 100 eV), and hence ion energy impinging on the substrate invariably increases, resulting in more damage to substrate.

An effective etching approach for HgCdTe using CH_4/H_2 plasma chemistry is electron cyclotron resonance (ECR) plasma reactor that produces low energy ions at low pressures (0.05–15 mTorr). High-density plasma is generated by matching the frequency of a microwave field (f = 2.45 GHz), with the cyclotron resonance frequency ($f_c = qB/2\pi m$) of the electron in a constant magnetic field (B = 875 gauss). At cyclotron resonance frequency the electron gains energy during the whole rotation cycle as shown below and the energy gained is proportional to the time between collisions, hence the ECR works only at low pressures typically below 10 mTorr. These plasmas are denser than RF plasma; high ion and electron densities (10^{13} electrons/cm^3) can be generated [2,29].

Figure 2 shows a typical ECR plasma reactor used for HgCdTe etching. It is composed of a high vacuum chamber; a microwave generator (f = 2.45 GHz), a sample holder connected to a RF generator (13.56 MHz); and magnets that produce 875 Gauss magnetic field. It is evident that resonance occurs only in a small confined region (microwave cavity) in the reactor where the magnetic field is uniform, and the sample holder is separated from the cavity by a considerable distance. The RF power controls the value of self-bias on the sample electrode. Thus, the ECR system has higher fractional ionization and lower ion energy than a RF parallel plate reactor. Another process utilizing similar system configuration is the low energy electron enhanced etching (LE_4). In this process, electrons at energies 1–15 eV and reactive species at thermal velocities are responsible for smooth damage free etching of HgCdTe [42].

Initial efforts towards ECR/ECR-RIE of MCT were made by Eddy *et al*. [2,10,35] who demonstrated fabrication of nanometer scale features in HgCdTe to study HgTe-CdTe quantum wires (40–70 nm wide) and quantum dots (~150 nm dia.). Different workers, for ECR plasma etching of HgCdTe, have used following variations of gas mixtures CH_4/H_2 [2,10,25], $CH_4/H_2/Ar$ [9,11,43–45], $CH_4/H_2/Ar/N_2$ [42,46] and Ar/H_2 [12,47,48].

Mass spectroscopic analysis of the etched products in ECR reactors using $CH_4/H_2/Ar$ chemistry, show peaks of each constituent element in the form of Hg, $Te(CH_3)_2$, TeH_2, and $Cd(CH_3)_2$. CH_4 is necessary for volatilization of Cd, H_2 is responsible for Te desorption while Ar serves to introduce

Table 3. Collected data for ECR etching of HgCdTe.

Ref.	Gas mixture	Chamber pressure (mTorr)	Microwave power (Watt)	RF power (Watt)	RF induced bias (Volt)	Etch rate (Å/min)	Characterization
27	H_2/Ar-100 sccm, upstream CH_4/Ar-20 sccm, downstream	4	750	50 0	–3 0	1500 500	Roughness ~40 nm, A.R. 5:1
14	CH_4/H_2/Ar 7:6:6 in sccm	2	300–400	–	No bias	2000	A.R. 5:1, sidewall angle 88°, RGA analysis, XPS, ellipsometry
29	CH_4/H_2/Ar 20/55/25 (% flow)	1	300	100	–50	–	SEM, Hall effect
28	$H_2/Ar/N_2$ -ECR source. CH_4-downstream	2	200	0–100	–20, 0	200–600	Extremely smooth surface
30	Ar upstream (80%) H_2 downstream (20%)	2	300	>100	0 to –635	CdTe/ CdZnTe/PR	Examined selectivity between PR and CdTe/ CdZnTe
15,31, 32	Ar/H_2 – 4/1	2	300	–	–55 to –65	–	Etch bias, anisotropy, resist features and IAD
9,2,13	CH_4 (18%)/H_2, total flow 15 sccm	1	250	–	–100	~100	A.R. 5:1, sidewall angles >88°
12	$5CH_4/17H_2/8Ar$	1	150	–	–100	ZnS/ZnSe/ CdS/CdTe	-Do-

physical component to the etching process it also acts as a diluent and stabilizes the plasma [45]. Etch parameters and data collected from different sources are reported in Table 3, it is evident that most of the times CH_4 and H_2 are introduced as downstream gases and Ar is introduced upstream.

Fabrication of multicolour detectors and APD's requires etching of high aspect ratio (A.R.) trenches, typically 10–15 μm deep and 3–5 μm wide, with good anisotropy to preserve high fill factors. ECR plasma etching is the most widely accepted technology for the purpose.

The issues to be addressed while developing the technology are:

- low roughness of the etched and sidewall surfaces,
- stoichiometry and electro-optical properties of the etched surface should be unchanged,
- excessive polymer deposition and redeposition of etch residue must be avoided,
- type conversion of the etched surface.

Process parameters that affect the above criteria are: the plasma gas-phase composition, total pressure, input microwave power, substrate bias, incident ion energy and substrate temperature. In addition, recent studies by Stoltz *et al*. [47–49], show the effect of photoresist sidewall angle, thickness; ion angular distribution (IAD) and ion energy distribution (IED) of the plasma on the A.R. of trenches. We shall investigate each parameter and its effect on final device properties, based on a survey of the available data.

4.3.1. Effect of gas input mixture

Figure 3 shows variations in intensities of different etch products as a function of gas input mixture (CH_4/H_2/Ar). $Cd(CH_3)_2$ and $Te(CH_3)_2$ emissions increase with CH_4 frac-

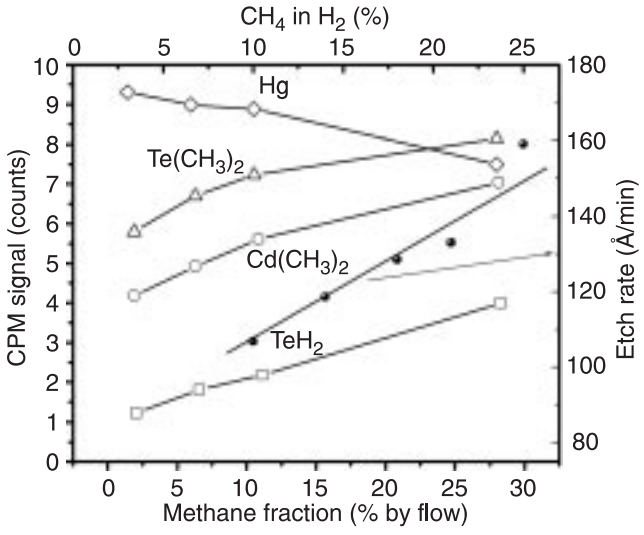

Fig. 3. Counts per minute of different etch products as function of CH_4 fraction in the gas mixture (CH_4/H_2/Ar). Plot of etch rate vs. vol. % CH_4 in H_2 gas mixture for the data collected from different sources at pressure of 2 mTorr, can also be seen. Etch rate increases with CH_4 fraction up to 20%.

tion because of increased flux of CH_3 radicals. TeH_2 signal also increases due to enhanced H concentration from dissociation of CH_4 and H_2. Etch rate of HgCdTe vs. vol. % CH_4 and/or Ar in H_2 gas mixture, for the data collected from different sources at pressure of 2 mTorr, is also shown. Etch rate increases with CH_4 fraction up to 20%. For higher methane flow ratio, a significant co-deposition of hydrocarbon polymer films is observed. This polymer film inhibits the etching of HgCdTe and increases surface roughness. Generally 10% CH_4 is suitable for moderate etch rate. Presence of CH_4 in ECR plasmas can cause polymer deposition on the sidewall of the etched film and plasma reactor walls. Polymer forming precursors are CH_2 and CH free radicals [50,51], which react to give unsaturated hydrocarbons (C_2H_2, C_2H_4) responsible for deposition of polymers. Polymer formation can be reduced by increasing DC bias on the substrate or by introducing CH_4 downstream [11].

A novel approach to reducing polymer deposition is introduction of N_2 in the ECR chamber in addition to H_2 and Ar mixture [46]. Atomic nitrogen produced in the ECR zone reacts with polymer precursors and unsaturated hydrocarbons to form volatile byproducts. It also reacts with atomic hydrogen (H) to form ammonia (NH_3), reducing H percentage and thus, enhancing methyl radical concentration needed for improved etch rate [47]. In this case no DC bias is needed for increasing the etch rate, which can damage the substrate. Design of a 20 μm pitch, two-colour, and triple layer structure is estimated to require a 15-μm deep trench, 3–5 μm wide at top [47,48]. This can limit etching of deep narrow trenches, required for next generation IR detectors. Stoltz *et al*. have extensively studied and modelled ECR etching of mentioned geometries using Ar/H_2 gas plasma, the mechanism can be called ion-assisted etching. Standard conditions for their ECR etching are listed in Table 3, where Ar (80 sccm flow) is introduced above the ECR zone, and H_2 (20 sccm flow) is injected downstream. Excited Ar^+ species generated in the ECR zone are used to dissociate H_2 while minimizing H^+ formation, since bonding energy of H_2 (4.5 eV) is less than ionization energy H_2 and H (15.4 eV and 13.6 eV, respectively). The etching species are primarily Ar ions and atomic hydrogen [12,46, 52,53], H reacts with Te and forms TeH_2 (volatile), and while Ar ions facilitate physical etching. A DC self-bias is applied to accelerate the positive ions generated in the ECR zone to extract Cd. The Hg volatilizes from the surface without any assistance [48,54].

4.3.2. Coupled microwave power

The microwave power determines the plasma flux incident on surface by controlling degree of dissociation and degree of ionization of the gas mixture introduced upstream in the chamber. Figure 4 shows the effect of input microwave power on peak intensities of etch products [10,44]. Microwave power increases the degree of ionization /dissociation of the etch species and does not affect the kinetic energy of the ions. The degree of ionization is most affected over the 200–400 W range, at 2 mTorr chamber pressure. Neutral methyl radicals (CH_3) and Ar dominate over the range of 200–300 W and ionized CH_3^+ and Ar^+ play important role over 300–400 W ranges. Hg product peak increases with microwave power due to enhanced sputtering, and TeH_2 flux increases because of increased dissociation of gas species. Dimethyl Cd and Te products show a slight decrease with microwave power beyond 300 W where flux of ionized radicals is enhanced. It is apparent that neutral methyl radicals are preferred over the ionized radicals for Cd/Te removal [44]. Therefore, microwave power less than 300 W is applied to almost all the ECR reactors used for HgCdTe.

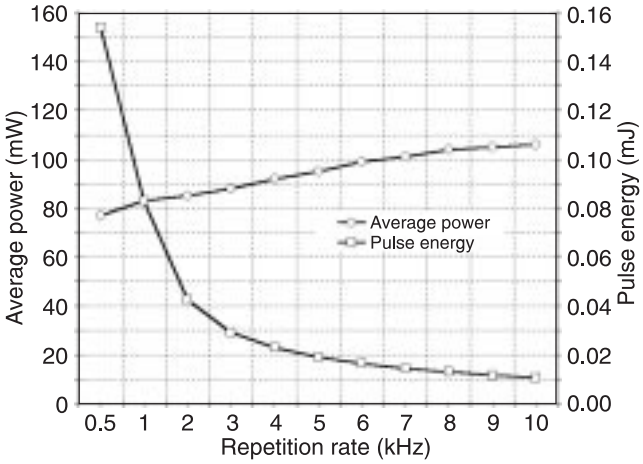

Fig. 4. The effects of input microwave power on peak intensity of etch products (CPM), reproduced from Refs. 11 and 47. Microwave power increases the degree of ionization of the etch species and does not affect the kinetic energy of the ions. The degree of ionization is most affected over the 200–400W ranges, at 2 mTorr chamber pressure.

4.3.3. Substrate (DC) bias (effectively incident ion energy)

The RF power applied to the substrate holder controls the value of direct current (DC) self-bias developed on the sample electrode. This DC bias is the most important factor in controlling the anisotropy and A.R. of trenches, as it controls the energy of incident ions and their angular distribution. Figure 5 illustrates the effect of DC bias on etch rate of HgCdTe, the data have been collected form different sources. The ion energy increases with DC bias and thus, increases the etch rate of HgCdTe, making the process ion assisted. It is observed that bias in the range of 75–100 V is desired for anisotropic etching. For bias greater than 100 V a transition to physical sputtering regime takes place [44]. Higher DC bias values also control the chemical passivation of sidewalls, since the ions responsible for trench etching acquire increased directionality [48,50].

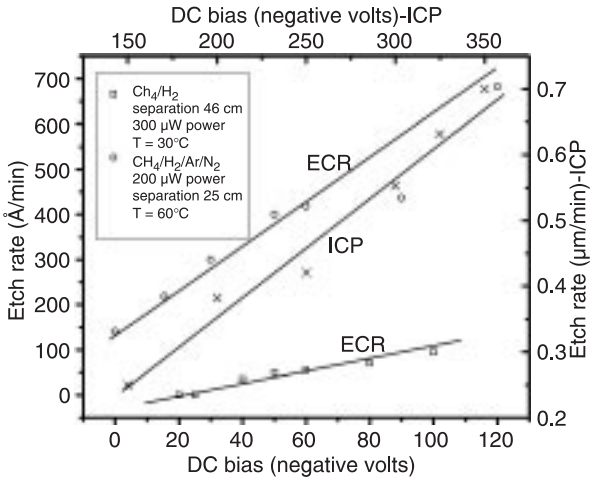

Fig. 5. Effect of DC bias on etch rate of HgCdTe, the data have been collected form different sources. Etch rate increases with DC bias; it is observed that bias in the range of 75–100 V is desired for anisotropic etching. For bias greater than 100 V a transition to physical sputtering regime takes place.

4.3.4. Total pressure

Process pressures less than 2 mTorr are desirable in ECR reactors. At higher process pressures, elemental Hg signal increases monotonically, due its high equilibrium vapour pressure. The metal alkyl etch products start to saturate at pressure >2 mTorr, because of reduction in fraction dissociated methyl radicals [44]. Thus, for higher pressures sufficient flux of CH_x cannot be maintained to promote surface etching.

4.3.5. Substrate temperature

Effect of variation in surface temperature of the wafer during etching has been studied by Eddy *et al*. [44]. For temperatures less than 50°C ion assisted surface chemistry is responsible for etching HgCdTe. Above 50°C, thermal chemistry dominates and an increase in Hg component due to thermodynamic removal mechanism is observed [50]. Other etch products are independent of temperature up to 50°C. In general, substrate temperature is kept at 5–30°C while etching.

4.3.6. Photoresist parameters and ion angular distribution (IAD)

Stoltz *et al*. have investigated and modelled ECR etching of HgCdTe trenches using Ar/H_2 gas chemistry. Their extensive studies showed that the trench geometry is a function of resist thickness; resist sidewall angle and DC bias input power. Salient features of their model are:

- HgCdTe trench formation depends on photoresist feature geometry [12],

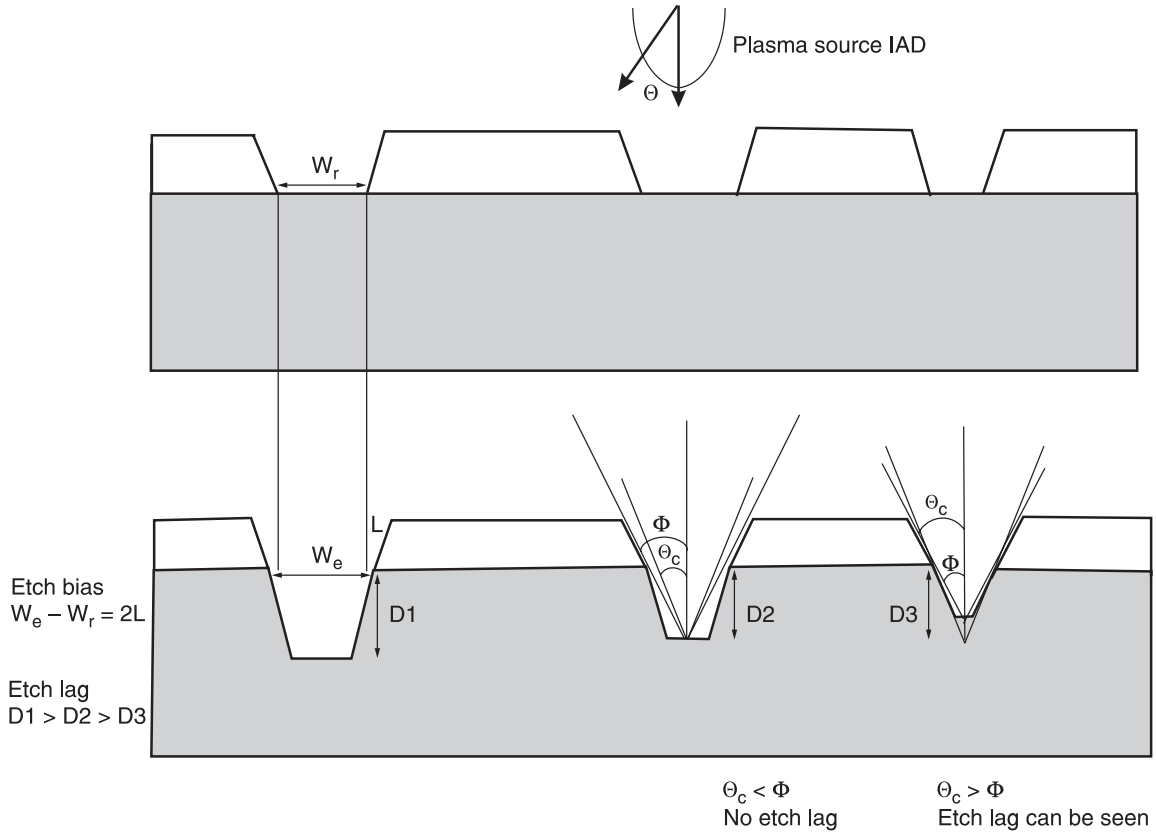

Fig. 6. Figure illustrating etch lag theory. The A.R. of a trench is defined by an angle Φ θ_c is the maximum of IAD. When $\theta_c < \Phi$, no etch lag occurs. When $\theta_c > \Phi$, fewer directional ions reach the trench bottom and etch lag is evident.

- etch bias for a HgCdTe trench is determined by lateral resist erosion rate [55]. As shown in Fig. 6, etch bias is defined as the degree of expansion of a feature beyond that defined in the mask and is given by $E_b = W_e - W_r = 2L$, where W_r is the printed resist pattern width, W_e is the width at top of etched trench (related to detector fill factor) and L is lateral under cut in trench,
- high aspect ratio trenches etch at a slower rate than low A.R. trenches. This is known as etch lag and complicates reticulation of trenches [56,57],
- a critical parameter that affects the etch bias and etch lag is the ion angular distribution (IAD) of the plasma [47,48,50].

Etch lag theory

The aspect ratio (A.R.) of a trench is defined as $A_r = D/W_e$, where W_e is the width at the top of an etched trench and D is its depth. For a given etch time, D is found to be a function of W_e (etch lag). Etch lag can be reduced by increasing DC bias on the wafer electrode. The ECR plasma chamber has it's own ion angular and ion energy distribution. The IAD is typically Gaussian-shaped and has a maximum at the centre ($\theta = 0$) from plasma perspective and θ_c is the twice FWHM of IAD. With reference to a point on the sample the IAD is peaked at a greater angle ($\theta > 0$). The etch lag effect occurs because of restriction in the number of ions able to penetrate the trench to the required depth. Let the A.R. of a trench be defined by an angle Φ as shown in Fig. 6, therefore $\text{A.R.} = (2\text{tg}\Phi)^{-1}$, then according to the etch lag theory the critical A.R. is related to the angle θ_c such that $\text{A.R.}_c = (2\text{tg}\theta)^{-1}$ [55,56]. When $\theta_c < \Phi$, then a large number of directional ions are able to etch the bottom of trench and no etch lag occurs. When $\theta_c > \Phi$, fewer directional ions reach the trench bottom and etch lag is evident.

The DC bias influences the plasma IAD. Keeping all other parameters constant, an increase in DC bias reduces the IAD and hence θ_c. Figure 7 is a plot of normalized trench depth vs. inverse aspect ratio (IAR), for different DC bias values, reproduced from Ref. 48. The etch depth has been normalized w.r.t. etch depth in an open area without lag D_o. It is representative of etch lag theory [47,48]. It is evident that at a given bias, there occurs a critical IAR value beyond there is no etch lag, the value of critical aspect ratio, A.R._c, is determined at a point where IAR becomes constant, it is also equal to the slope of the fitted line [48]. For $\text{A.R.} < \text{A.R}_c$ the etched depth approaches D_o and no etch lag is observed. For $\text{A.R.} > \text{A.R}_c$, $D/D_o < 1$ and presets etch lag phenomenon. The value of A.R_c increases with input DC bias because of reduced IAD and increased ion energy.

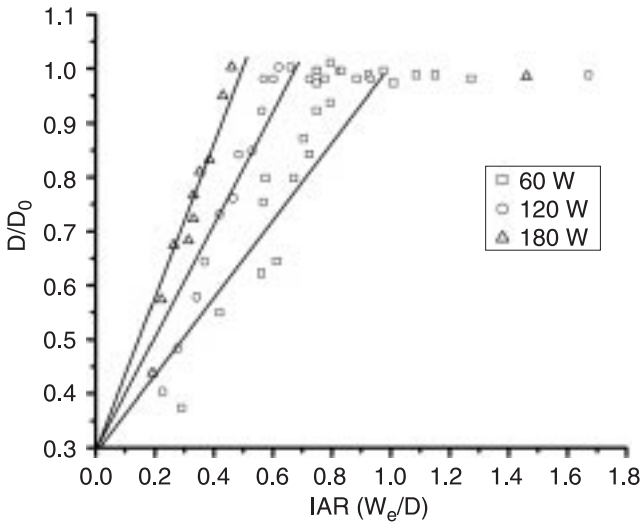

Fig. 7. Plot of normalized trench depth vs. inverse aspect ratio (IAR), for different DC bias values, reproduced from Ref. 46. It is representative of etch lag theory.

Lateral resist erosion model

The aspect ratio of a trench depends on etch bias and anisotropy [47]. Both the factors can be improved using thick (5–10 μm) steep sidewall resist features (80–85°). Anisotropy is defined as $A = D/L$, this leads to relation $W_r = W_e - 2D/A$ [12]. Thus, knowing A and desired A.R., proper mask features can be designed for delineation of small closely spaced pixels needed for high fill factors.

The etch bias is determined by lateral resist erosion rate, which in turn is dependent on resist sidewall angle and ion angular distribution that causes lateral resist erosion [47]. For a constant resist feature geometry, the etch bias depends on the DC bias applied to the wafer electrode [47,55]. DC bias controls the IAD and energy of incident ions. According to Jansen's IAD theory [57], the vector angle responsible for resist erosion is $\Psi = 90 - \theta_c$. The value of θ_c decreases as a function of increasing DC bias input power, therefore, lateral resist erosion vector angle $\Psi \rightarrow 90°$, thus, lateral resist etch rate decreases, leading to an anisotropic etch. Lateral resist erosion decreases dramatically at the bias above 180 W because of resist hardening due to high-energy Ar ion bombardment [49]. For long etch times, steep sidewall, thick resist films reduce the lateral erosion rate and decrease the etch bias, because time for resist corner rounding to reach the HgCdTe will decrease. However, increase in resist thickness does not affect the critical aspect ratio.

It has been found in a separate study that lateral resist erosion is primarily due to a broad range of large incident angle ions [50]. Decreasing the DC bias can reduce this distribution. The IAD responsible for HgCdTe etching is a narrow range of near normal incident ions [50]. Hence, loss of large angle, low energy ions in resist erosion does no alter A.R_c and etch lag. Thus:

- increasing DC bias input power leads to higher aspect ratios,
- etch lag is independent of a thickness of resist,
- use of hardened resist makes dramatic changes in final trench profile.

High A.R. trenches have been etched for fabrication of two-colour detectors [47]. Thick (10 μm), steep sidewall

resist ($\theta = 85°$) etched at 180W DC bias, W_e = 2.91 μm, W_r = 2.66 μm, D = 15.74 μm. Thus, trenches with widths less than 3 μm and depths greater than 15 μm have been achieved by applying 180 W DC bias. This width will enable delineation of small, closely spaced pixels required for high-resolution detector arrays. This depth will also enable the optical isolation pixels in the multilayered structures, needed for two and three colour detectors and APD's.

4.4. Inductively coupled plasma etching

Alternative high-density plasma etching technique, preferred in the semiconductor industry for manufacturing applications is the inductively coupled plasma (ICP) etching. Raytheon Vision Systems is actively developing this high-density plasma etching technique for productions of two-colour FPA's. In the ICP technique, an inductor coil is wrapped around or above the roof of the dielectric vessel (Fig. 2). Plasma is generated by application of RF power to the coil. This is a preferred technique where larger wafer dimensions are to be processed with high uniformity, and also provides greater automation capability than ECR plasma [52–54]. It was found that ICP etching is capable of producing up to a factor of 5 reduction in lateral mask erosion during, thus, showing improved etch uniformity and less significant etch lag effects [59,60].

A study was performed to investigate the effect of chamber pressure, DC self-bias and ICP source power on trench etching of 30 μm unit cell FPA's using 4 μm trench width. With increasing DC bias, the ion bombardment energy, at the wafer surface, increases and contributes to greater etch rate. At fixed DC bias and source power, the etch rate increases with chamber pressure, because of an increase in available gas molecules for ionisation and etching. With increase in source power, the ionization of gases increases and etch rate increases.

A comparison of ECR and ICP etch techniques showed that ICP is capable of providing superior uniformity over large wafer diameters than ECR systems [59].

4.5. Ion beam etching

Ion beam etching is a process by which a substrate surface is slowly eroded by bombardment with stream high-energy (200–1500 eV) argon ions. Etching takes place if the momentum transfer to the substrate atom is sufficient enough to be vectored away from the surface [61,62]. Ion beam etching systems consist of a plasma source to generate the ions (Kaufman ion source), the extraction grids from ion extraction from source and substrate holder. This is a purely physical process that is capable of highly anisotropic pattern transfer, but its selectivity is poor and can induce mechanical and electrical damages. Ion milling is being used to delineate n-HgCdTe photoconductor devices and fabricate via interconnects in n-HgCdTe based VIMIS devices [63]. However, its use for mesa delineation of photodiodes is limited because of the extent of damages and type conversion of p-type material to n-type to large depths [64,65]. Ion beam milling is primarily being used fabricate p-n junctions in MBE/LPE grown HgCdTe [66,67].

5. Etch induced damage

While developing a dry plasma etching technology for HgCdTe, there are certain aspects of the materials that need to be taken care of:

- conductivity type conversion,
- stoichiometry changes and creation of defects,
- surface roughness,
- polymer deposition.

The low damage threshold of HgCdTe is due to weak Hg-Te bond and low volatility of CdTe component. A physical component in dry etching is required for anisotropic mesa profile and achieving a stoichiometric surface. A certain level of ion induced reaction is necessary for etching HgCdTe to overcome low volatility of Cd and assist in desorption of etch products form the surface [11,68–70]. Ion bombardment during dry etching can modify the electrical and optical properties of HgCdTe [71,72].

Both ion milling and RIE cause damages to HgCdTe during etching. Ion milling of HgCdTe results in creation of extensive structural defects, type conversion of p-type HgCdTe extending to large distances (~200 μm) for short process times [64,73–75] and produces long-range isotropic damage in n-type HgCdTe [63]. Reactive ion etching of HgCdTe using CH_4/H_2 discharge, is done at the process pressures of 100–400 mTorr and ion energies are > 100 eV. These systems induce type conversion and damages in the processed devices, particularly of p-type material [73].

A study of spatial changes in electrical characteristics of HgCdTe photoconductive (n-type) and photovoltaic (p-type) fabricated by RIE system was performed by Smith *et al*. [72,74] and compared to wet chemical processing using Br_2/methanol. They performed laser beam induced current (LBIC) measurements to characterize electrically active impurities/defect clusters, material in-homogeneities, junctions etc. The comparison results are reported in Table 4. Wet processed devices show a superior performance (responsivity, detectivity and noise) to those that have undergone dry plasma etching. However, the RIE induced type conversion in extrinsically doped p-type and intrinsically doped n-type HgCdTe can be removed by low temperature mercury annealing [76–78,80,81].

ECR etching of HgCdTe using low energy Ar ion bombardment has a sputter component at high DC bias values and results in increased Hg removal [44]. The damage depth due to sputtering has been estimated to <10 nm at operating bias voltage [48]. RHEED, LEED analysis of ECR etched (211) surface showed a crystalline surface unlike the amorphous surface observed in III-V semiconductors, but a twinned and faceted surface was observed, all other defects recombine to give a crystalline surface [50,82]. Planar surfaces of etched HgCdTe have been analysed for

Table 4. Etch induced damage for different processes.

	Type conversion	Electrical/device properties	Defects/surface
RIE (CH_4/H_2 plasma)	Lateral type conversion beyond the mask perimeter. n- to n^+-type 5 μm in extent p- to n-type 50 μm in extent in the masked region, and type conversion extends vertically down to substrate	Responsivity reduced by a factor of 3 (photoconductor) Effective minority carrier lifetime reduced to 3.7 μs Noise voltage 6.5 $nV/Hz^{1/2}$ 1/f knee frequency ~2 kHz $D^*=2.5\times10^{11}$ $cmHz^{1/2}W^{-1}$, background limited	Extended defects are created in n-type HgCdTe, responsible for increase in donor density [55] Creation of Hg interstitials in p-type HgCdTe that diffuse into the substrate to annihilate acceptor vacancies and kick out of extrinsic p dopants
Wet chemical	No type conversion	Responsivity is better by a factor of 3 Effective minority carrier lifetime 10.5 μs Noise voltage 50 $nV/Hz^{1/2}$ 1/f knee frequency ~10 kHz $D^*=1.0\times10^{10}$ $cmHz^{1/2}W^{-1}$, not background limited Fill factor of 40%, large pixel pitch (~50 μm)	Degree of lateral undercut limits the minimum feature size and detector density Residual Te
Ion beam milling	Extent of type conversion is quite large (~2.5–200 μm deep) depending on Ar ion energy	Highly anisotropic etch, PC detectors	Trenching and redeposition, extended defects
HDP (ECR)	Approximately 0.35–0.7 μm of the p-type surface is converted to n-type with low electron mobility (~700–1000 cm^2/V-sec), this converted layer can be removed by chemical etching [65]	Reverse breakdown voltage ~(–0.7) volt and good I-V performance. Anisotropic profiles Good quality diodes with high impedance (>10 GΩ) Pixel pitch can be reduced to 20 μm. High fill factor ~80%. Noise voltage 13$fA/Hz^{1/2}$	Faceted and twinned surface at high DC bias values. Surface roughness is <10 nm at operating bias voltages
HDP (ICP)	No reports on type conversion, as the ion energy and process pressure are quite low	No electrical damage, superior uniformity over larger wafer diameters than ECR systems. Small pixel pitch with high fill factors can be achieved	

changes in stoichiometry and transport properties [15,82]. But the properties of sidewall of the mesa may be different and are difficult to characterize. Mesa sidewall damage, n-type doping variations, introduction of additional minority carrier recombination centres etc. can degrade detector performance. Reverse bias I-V characteristics of 30 μm unit cell HgCdTe diodes of various trench geometries were measured at 78 K [65,82]. The results indicate that diodes exhibit a good performance (break down voltage of –0.7 V) with high impedance. The more narrow trenches or trenches that have been etched to a greater depth with etch lag effects, show a degradation in I-V characteristics with smaller breakdown voltages and increased reverse current.

The noise performance of the dry processed detectors (any technique), as seen from Table 4, is lower than wet etched devices [65,71]. However, dry processing, particularly HDP etching is capable for reducing pixel pitch and dramatically improving fill factors needed for high-density detector arrays. Hence for a given unit cell design parameters (etch depth, width, mesa profile and process time), the dry etch process has to be optimized to give high performance diodes.

6. Conclusions

Almost all the wet and dry etching techniques, used for HgCdTe etching, have been reviewed with emphasis on ECR etching technique. Wet etching is isotropic and needs high etch bias. RIE of HgCdTe invariably results in type conversion and surface roughening at the sidewalls of masked features. RIE has been rather utilized in p- to n-type conversion and inducing stoichiomeric variations for fabricating photodiodes and other novel device applications.

The present and future generation devices require high aspect ratio mesa isolation for large density arrays with minimum etch induced changes. These requirements are met by using state of the art dry processing techniques such as ECR, ICP and LE_4 (HDPE). Most aspects of ECR technique such as effect of microwave power, gas input mixture, DC bias and effect of IAD and IED on trench geometry have been studied from available literature and are reported here. The process parameters for different techniques and applicability of these techniques to HgCdTe devices are listed in the tables. The data have been collected from different sources.

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