OPTO-ELECTRONICS REVIEW **14**(1), 79–86

4×288 readouts and FPAs properties

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Analysis of four types 4×288 designed and manufactured readouts is presented. All the readouts have the direct injection input circuit with the circuits incorporated that allows testing procedure of readouts without the photodiodes attached to readout circuits. TDI registers have three delay elements between neighbouring inputs. Some characteristics of 4×288 FPAs with mercury-cadmium-telluride (MCT) arrays are presented too. Analysis have shown that in spite of different constructions of four readout types, different numbers of outputs and external service, rather similar parameters of FPAs have been obtained. Detectivity values measured for all 4×288 FPAs at operation temperature T ≈78 K with skimming mode included and background temperature T_b ≈295 K were in the range $D^*_\lambda \cong (1.2–1.7)\times10^{11}$ cmHz$^{1/2}$/W.

Keywords: MCT, readouts, FPAs.

1. Introduction

Today, FPAs on the merury cadmium telluride (MCT) base are the most widespread devices for 3–5 μm and 8–12 μm IR region and they are operating practically with ultimate performance [1,2]. Since the early ninetieths of the last century, high resolution scanned arrays with time delay and integration (TDI) function and signal processing [first with charge coupled devices (CCD) for readouts] within the focal plane for standard TV formats resolution using mechanical scanning and odd and even line interlacing (576×768 European format) have been proposed [2,3]. This type of FPAs was widely adopted. Here, our experience in design of 4×288 readout devices (ROICs), fabricated by different technologies, and some features of MCT FPAs are discussed.

For 3–5 μm region, staring matrix arrays with comparable dimensions to TV format and even in the case of lower quantum efficiency have clear advantages over scanning arrays even with TDI function [4,5] but for 8–12 μm spectral region they are of comparable effectiveness and scanning arrays can be more cost effective. Moreover, in 8–12 m region in matrix arrays with small diffraction limited pixel size, crosstalk between neighbouring sensitive pixels (due to diffraction limit and quality of optics manufacture, and also due to diffusion processes of photo-generated carriers) can play an important role in image quality. In scanning arrays (Fig. 1), the distance between sensitive elements are larger and the effects mentioned influence the FPA performance less. Also, in the images obtained by scanning arrays information losses are less, as there are no energy losses in radiation falling down on arrays, as respective losses at formation of electrical signals. These losses exist in matrix arrays because of clearance space between neighbouring sensitive elements in them (as a rule, the clearance space between the elements should not be less that the operation wavelength to avoid the optical crosstalk). Also, because of matrix filling smaller than 100%, the losses of high frequency components of the optical signal exist too [6].

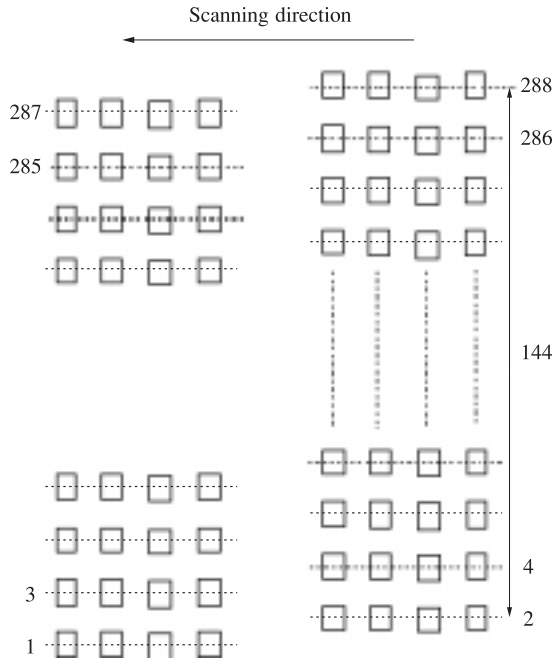

Fig. 1. Schematic arrangement of 4×288 MCT photodiode array with TDI function.

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2. ROICs basic characteristics

Four different types of ROICs for 4×288 MCT arrays, with the dimensions of photodiode sensitive cells of 25×28 μm were designed and manufactured. For 4×288 format readout circuit, different technologies and electronic components can be used but in any case the circuit should be composed according to the block-diagram model shown in Fig. 2.

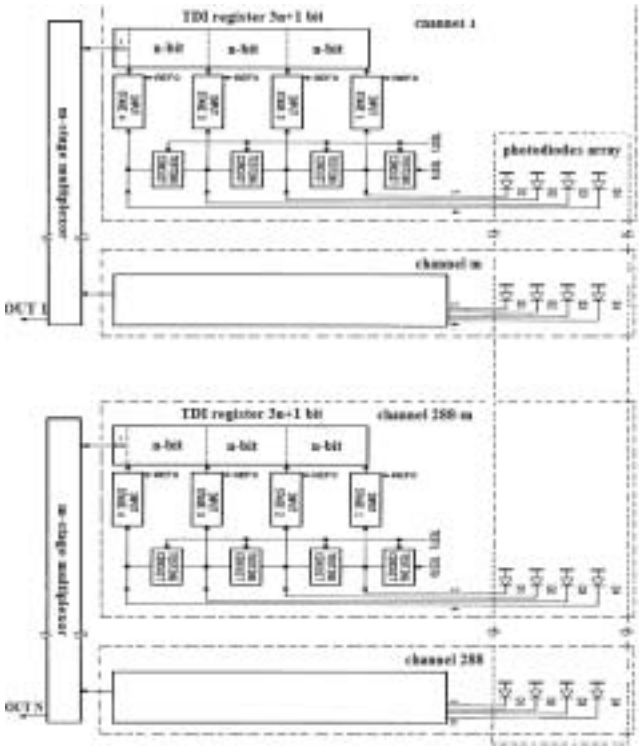

Fig. 2. Block-diagram of 4×288 ROIC.

The number of outputs N depends on resources of instrumentation used for signal managing. ADC resources define the multiplexor capacity. The number of TDI stages between the inputs is chosen from the needs of space resolution. In the circuits stated, three stages were chosen.

For manufacturing of 4 readout types, three different technological roots were used:

- 2.5 μm n-MOS (n-type metal-oxide-semiconductor) + CCD (charge coupled devices) technological process with two levels of polysilicon electrodes and one metallization level. Four-inch boron-doped p-type <100> Si wafers with resistivity of 12 Ω cm were taken for the process. The large scale integration (LSI) circuit under the consideration consists of MOS transistors with gates from first and second polysilicon level and CCD cells with buried and semi-buried channels [7]. The under-gate dielectric is a thermally grown SiO_2 layer with the thickness of about 500 A with threshold voltage of ≈ 0.3 V.

  Multiplexers were designed for CCD technology with a buried channel. To simplify the external control circuits, the CCD cell with asymmetric potential well was used. The storage charge region is created by phosphorus ion implantation (D = 0.16 μC, E = 100 keV) into the under-gate region from polysilicon first level. To fabricate the barrier regions under the gates from polysilicon second level there is used the second boron implantation (D = 0.12 μC, E = 60 keV) which compensates the part of implanted phosphorus. The resulting depth of potential well for storage of the information charge was about ΔV ≈5 V, and multiplexer charge capacity Q was equal to Q = 2.5 pC.

  Shift register of TDI with four inputs of information charge is also designed as CCD cells with asymmetrical potential well. To increase its charge capacity, the technology of semi-buried channel [7] was used, charge capacity regions under first polysilicon level were manufactured by phosphorus ion implantation at the same time with manufacturing the capacity regions in multiplexer and in barrier region there is executed the addition boron implantation with D = 0.05 μC and E = 60 keV that increases the depth of the potential well to $\Delta V \approx 8$ V. The charge capacity of the TDI register output bit was about Q = 2.4 pC. Important for FPA operation dead pixels deselection function was not possible to include to this type of ROIC:

- another design provided for operation of CCD registers four-phase control and, because of that, the barrier region was not formed. Also, the technology of CCD fabrication with surface channels was used. In this case, the procedure of buried channel under the polysilicon gates was also excluded.
- 2.0-μm CMOS (complementary metal-oxide-semiconductor) +2.5-μm CCD (charge coupled devices) technological process with two levels of polysilicon electrodes and two metallization levels was elaborated. Si wafers with the same electrical characteristics were taken for the process. Under-gate dielectric is a thermally grown SiO_2 layer with the thickness of 350 A and threshold voltage (without doping) of $\Delta V_{th} \approx 0.15$ V.

  Earlier, for rather similar purposes in 4×480 TDI arrays, the multi-crystal concept was used [8]. In this case, crystals which include the interface circuits of charge trans-impedance amplifier (CTIA) type, reconfigurable handling capacity, and deselection devices, were manufactured by 1.5 μm CMOS technology. The crystals of signal processing, which include the circuits of TDI, amplification and signal charge processing, and also the CCD clock pulses former, were manufactured by 1.5-μm p-channel technology.

  The technology used here differs from the standard digital CMOS route (so-called, one-pocket technology) by two additional operations: electrodes formation from the second level polysilicon, and formation of buried channel in the region of CCD charge transfer. This technology needs special operations availability, which allows to realize both analogue and digital elements. Moreover, it requires different designs and technologi-

cal restrictions for analogue and digital parts of the circuit. But at the same, one can use less severe design rules (not better than 2.0 μm for CMOS part and 2.5 μm for CCD part) to obtain similar characteristics compared to those manufactured for pure CMOS 4288 readouts with design rules 1.2 μm or better.

The circuits under the consideration consist of MOS transistors with gates from first and second polysilicon level and CCD cells with buried and semi-buried channels. The direct injection transistors are designed as MOS-transistors with induced channel (the width-to-length ratio $W/L = 3$) with first polysilicon level gates. The under-gate dielectric is a thermally grown SiO_2 layer with the thickness of 350 A and threshold voltage of approximately 0.1–0.3 V.

To avoid the dead pixels influence on FPAs operation, the deselection function for TDI 4×288 multilinear MCT photodiode array was included at the readout circuit level. The pixel area is about 2500 square microns (pixel dimensions ≈56×43 m). Here, also direct injection (DI) transistor should be placed. In this situation, it should be taken into account that to ensure DI transistor processing at subthreshold regime at sufficiently large currents and to decrease the dependence of drain voltage, the dimensions of direct injection transistor should not be diminished greatly.

- standard 1.2 μm CMOS technological process, which includes two levels of polysilicon electrodes and two metallization levels, was also elaborated.

Comparative parameters of the technologies used are presented in Table 1.

3. Comparative description of ROIC basic assembly units

In all circuits, the unit cells with DI were chosen to improve the coupling between PV detector and readout devices, as it is typically done for 8–12 μm region [9]. DI transistor characteristics are important for read-out device performance. To ensure the minimum characteristics dispersion for direct injection transistor, "natural" transistor was used which did not include additional operations of channel doping. Besides, DI transistor of rather large area was designed. It ensured, the characteristics deviation within 10 mV in all the circuits designed. For maintenance of linear transfer characteristics, transistor with the long enough channel length ($L = 6$ μm) to exclude dependence of direct injection transistor current on drain voltage was chosen.

For carrying-out the testing procedure, the circuit used in Ref. 7 was employed. CMOS ROICs were designed and manufactured by 1.2-μm technological process, testing transistors were connected up to inverse output of trigger-latches, ensuring deselection of dead elements. To provide the possibility of testing, the circuit for identity of channel characteristics, one should supply low resistance of lead wire bus, otherwise additional voltage drop will lead to additional channel non-identity.

Analogue input circuit (Fig. 3), which was used in n-MOS + CCD and CMOS + CCD technologies, provided several operation modes (skimming, partition, anti-blooming) to change the input effects. Changes of storage capacity in this cell is carried out by voltage changing supplied to the capacities C1 and C2.

As the input matching circuit (Fig. 4) it was used the one that includes direct injection transistor, accumulation capacitors, additional gates which provide antiblooming function, additional transistors for testing, and partitioning and skimming.

High identity demands to these circuits predetermine the necessity of their manufacturing without use of additional doping of undergate regions and with relatively large dimensions. Thus, in this construction, the direct injection transistor is realized with the channel width $W = 18$ μm and the channel length $L = 6$ μm. Deselection control is realized

Table 1. Some comparative parameters of technologies used for fabrication of 4×288 ROICs.

Parameters	Type of technology		
	2.5 μm (NMOS + CCD)	2.0 μm CMOS + 2.5 μm CCD	1.2 μm CMOS
Wafer	four-inch boron-doped p-type <100>12 Ω cm	four-inch boron-doped p-type <100>12 Ω cm	four-inch boron-doped p-type <100>12 Ω cm
Number of photo-masks	9	14	11
Thickness of under-gate dielectric	450 ±50 A	350 ±50 A	250 ±15 A
Threshold voltage nature transistor	0.3 ±0.15 V	0.3 ±0.15 V	0.15 ±0.05 V
Channel width	2.5 μm	2.4 μm	1.6 μm
Minimum bus width plus space poly Si-1	9 + 3 μm	7 + 2.5 μm	1.5 + 1.2 μm
Width plus space poly Si-2	9 + 3 μm	7 + 2.5 μm	not used
Width plus space μmetal-1	5 + 2.5 μm	4 + 1.6 μm	2.4 + 1.8 μm
Width plus space metal-2	–	4 + 2.0 μm	3 + 1.8 μm

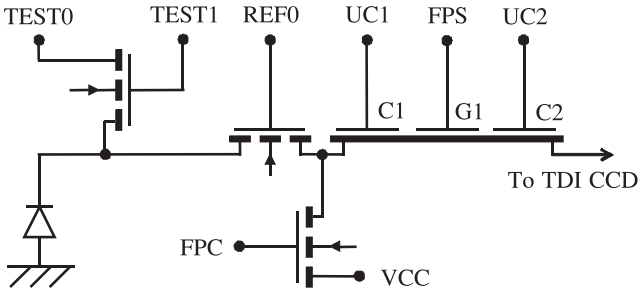

Fig. 3. Schematic representation of the matched input circuit. TEST0 is the input for CCD testing, TEST1 is the transistor, which opens the input of TEST0, REF0 is the transistor which sets the operating point (bias) at photodiode, UC1 and UC2 are the accumulating capacities, FPS is the gate, which control the skimming and partitioning regimes, VCC is the supplied voltage, FPC is the antiblooming electrode.

by C2 electrode by its grounding or applying the bias voltage (with TTL level). It provides chip space saving in comparison with latches application.

There are several possible deselection solutions but here the following one was used: dead photodiode is a little bit biased, the bias level provides the antiblooming gate, the current of which is connected to power supply that diminishes its influence on the neighbour elements. On the other hand, there are no additional elements in this circuit. The maximum input charge in the circuit designed is up to 3.5 pC.

TDI of charges in the channels is realized at CCD registers. As each stage of TDI CCD register should contain the charge package from four photodiodes (in conditions when bidirectional scanning is used) they are located behind the

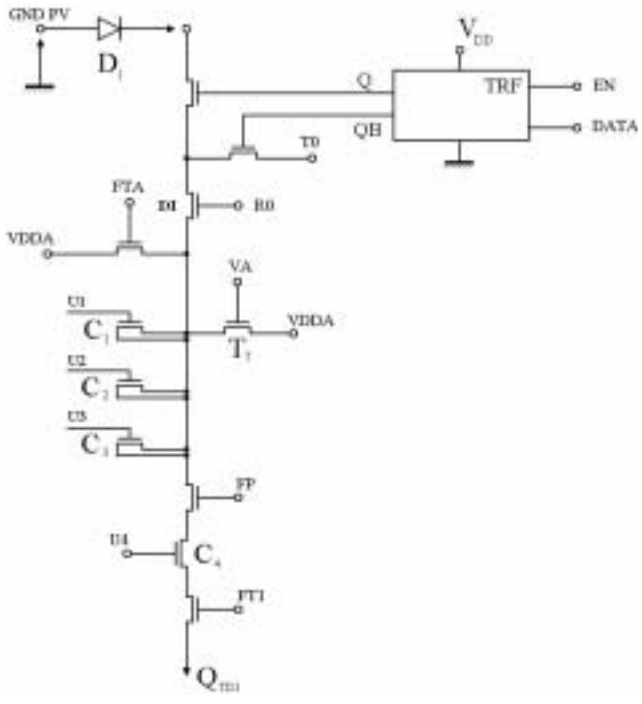

Fig. 4. Digital input circuit.

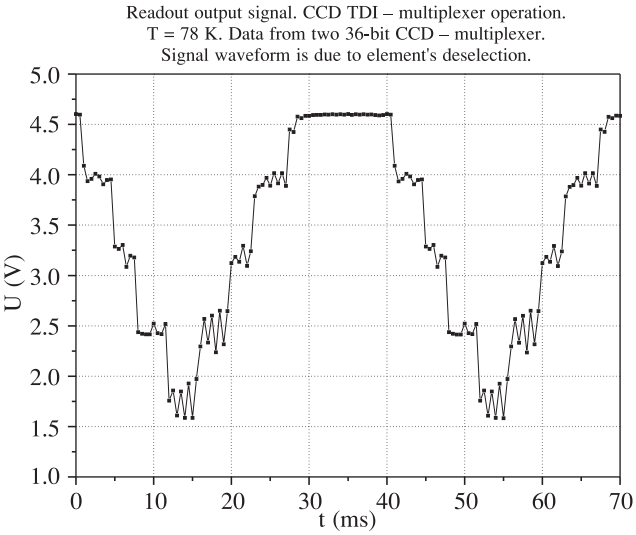

Fig. 5. Active elements for 2×4×144 readout mapping performed with the help of deselection function.

region of contacts to photodiode array. The area which occupies the stage of TDI CCD register is 56×600 μm. TDI register is realized by the technology of semi-buried channel [7] or surface channel, the cell dimensions are 48×16 microns, that allow to place the charge up to 3.5 pC. The example of deselection operation mode in one of the channels of 4×288 readout circuit is shown in Fig. 5. In this figure, the readout output signal from two 36-bit CCD multiplexers is shown. Each point corresponds to the output signal from one of 288 photosensitive elements. Due to the performed deselection, the photocurrent from one, two, three or four photodiodes contributes to overall output signals.

For silicon TDI CCD registers and CCD multiplexers, the common problem appears, i.e., a decrease in charge transfer efficiency with temperature decrease due to electrons capturing by impurity levels in a silicon gap. Nevertheless, it should be noticed, and it was shown experimentally, that this problem does not influence sufficiently the resulting device characteristics at cryogenic temperatures. At CCD register length used, the temperature decrease leads to transfer efficiency coefficient decrease, and channel crosstalk increase. TDI operation mode is rather similar in appearance to that one shown in Fig. 5 for deselection operation mode.

More serious is a problem of CCD voltage supply decrease (in this case from 10 V to 5 V). This requires obtaining of shallow buried arsenic doped channels. However, the experiments showed that the charge transfer efficiency changes substantially with temperature decrease for shallow buried channels created by arsenic doping. Therefore the voltage amplitude of power supply clock pulses should be relatively large (about 10 V) in the ROICs designed.

The typical charge-voltage transfer characteristics measured at $T = 298$ K and $T = 78$ K are shown in Fig. 6. These measurements were performed using test transistors for photodiodes current imitation. It is seen that the designed

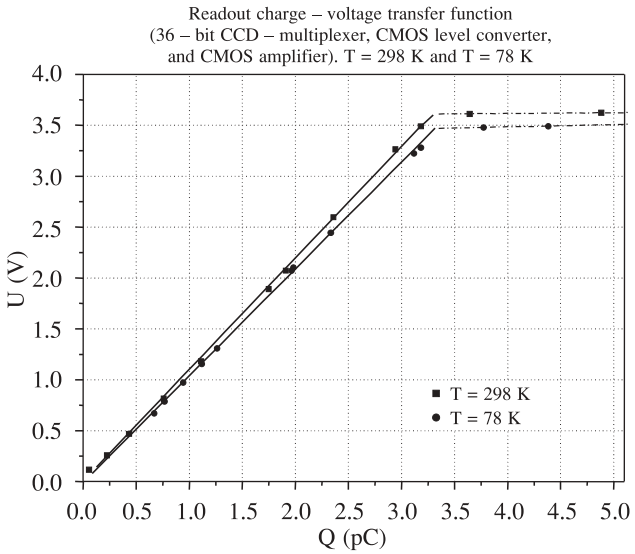

Fig. 6. Charge-voltage transfer characteristics at $T = 298$ and $T = 78$ K.

circuit demonstrates good linearity at the voltage level up to 3.5 V. Maximum charge capacity measured is up to 3.5 pC.

One of the most important parameters of the readout circuit that operates in cryostat cold zone is a power consumption. The restrictions with which power consumption of the output circuits do not exceed 10 mW per one output (with total power consumption calculated near 40 mW). Total consumption power measured is about 50 μmW at T = 298 K and 70 mW at T = 78 K. The calculated value of dynamical range is 84 dB and the measured one is 75 dB because of a limitation connected with restrictions of measuring equipment.

In the circuit, fabricated by CMOS technology, "digital" input circuit was used (Fig. 4). In this type of the circuit, only one regime is realized (partition). The input capacity was changed by a digital code which was supplied to U1, U2, U3 buses, switching on or switch off C1, C2, and C3 capacities.

TDI procedure in all the designed and fabricated circuits is realized by analogue procedure, using charge storage and summing in CCD elements. The number of TDI stages was chosen as $n = 3$, and total number of TDI register stages is 10. For this purpose, in CMOS circuits, a CCD version is used, that is "bucket brigade". This is a sole CCD type which can be realized in standard CMOS technological route. Such kind of a cell has low charge transfer coefficient, but for TDI registers it is not principal because of their short length, low frequency transfer, and summing equal to charges at 4 inputs. Favourable feature of such a cell is practical absence of transfer degradation effectiveness at cryogenic temperatures. In ROICs with CCD parts, the included TDI function is designed as various CCD cells: two-phase, four-phase, buried channel, semi-buried channel, and surface channel. In the last case, the structure of TDI register was simpler. Basic efforts at design and fabrication were directed to increase in charge handling capacity, which limited the value of charge summed and thus, a dynamic range.

In CCD ROIC versions, information multiplexing was carried out also with different types of CCD registers. Parallel charge injection in every multiplexor bit provided end-to-end processing of information charge without intermediate charge-voltage conversion. Charge-voltage conversions are executed only at the multiplexor output. This allows to get high channel uniformity. Charge-voltage conversion is realized at CCD output at floating diffusion region. As an output stage in n-MOS-CCD ROIC versions, a source follower cascade was used. To improve transformation linearity in CCD-CMOS ROIC version, a converting CMOS amplifier was applied.

At substantial structure simplicity and use convenience CCD multiplexors possess one considerable fault. Decrease in efficiency transfer at cryogenic temperatures results in increase in interchannel interaction. As a rule, this interaction is within 2–5%, but in some cases (at displacement of two the most contrast points at end stages of register-multiplexor) it can reach 20%.

In CMOS ROIC version, the charge-voltage conversion takes place at the output of TDI register. For this purpose, a charge sensitivity amplifier is used, from which information in the form of voltage is transmitted into channel amplifiers where it is stored for a multiplexing time. Digital decoder connects channel amplifiers to output amplifier in series.

If compare the noise characteristics of these two types of multiplexing, it can be concluded that they are rather similar. The dynamic range in both cases exceeds 80 dB. In CMOS circuit, the basic weakness is a substantial difference in a constant signal, corresponding to dark current, it can reach 200 mV.

Basic parameters of the designed ROICs are presented in Tables 2 and 3.

4. FPAs properties

In all circuits, the designed and manufactured MCT arrays and Si readouts were hybridized by cold welding In bump technology. Because of TDI function from four photosensitive diodes in the chain of 4×288 array, the output information from 288 channels are formed from 1152 sensitive elements. The output 288 information signals are grouped by 72 channels and were brought out by four analogue outputs at maximum frequency 4 MHz. Some back-side illuminated arrays properties were investigated at $T = 78$ K. Typical spectral sensitivity curve of three photodiodes in one of the arrays tested is shown in Fig. 7. The non-uniformity of the chemical composition over an area of 1 cm^2 does not exceed $\Delta x = \pm 0.001$ that provided high uniformity of cut-off wavelength characteristics [10].

Figure 8 shows the dependences of differential resistance in three typical photodiodes in one of 4×288 array which demonstrates high and relatively homogeneous im-

Table 2. Basic parameters of ROICs.

Parameter	ROIC type		
	NMOS-CCD	CMOS-CCD	CMOS
Structure(N×m)	16×18	4×2×36	4×72
Input stage	DI, analogue 2 capacitor stage with anti-blooming and background skimming	DI, analogue 2 capacitor stage with anti-blooming and background skimming	DI, digital 2 capacitor stage with anti-blooming and background skimming
Testing stage	controlling testing transistor	controlling testing transistor	testing transistor include in trigger deselection
Pixel random deselecting	no	yes	yes
TDI	CCD register 4-input 3-bit between input 10-bit total	CCD register 4-input 3-bit between input 10-bit total	reverse BBD register 4-input 3-bit between input 10-bit total
Multiplexer	18-bit CCD	36-bit CCD	sample and hold amplifier
Output stage	source follower	operation amplifier	operation amplifier
Additional functions	no	yes, pixel random deselecting	yes, pixel random deselecting, reverse TDI scan, 8-range gain adjustment, bypass testing, main-clock based internal time sequence

Table 3. Parameters of ROICs.

Parameters	N-MOS-CCD	N-MOS-CCD		CMOS-CCD	CMOS
	2-phase	4-phase buried channel	4-phase surface channel		
Maximum input charge integration capacity	6.4 pC	6.4 pC		4.0 pC	4.48 pC
Using range of adjustment input capacity	0.2–5.0 pC	0.2–5.0 pC		0.2–4.0 pC	8 digital stage 0.56, 1.12,…4.48 pC
Charge handling capacity of TDI register	2.0 pC	2.2 pC	2.6 pC	3 pC	2.2 pC
Output rate of video Signal	2 MHz	2 MHz	2 MHz	4 MHz	5.5 MHz
Maximum output signal	≥ 5 V	≥ 5 V	≥ 6 V	≥ 3 V	≥ 2.5 V
Dynamic range	≥ 67 dB	≥ 70 dB	≈ 70 dB	≥ 70 dB	≥ 77 dB
Noise	≤ 2 mV	≤ 2 mV	≤ 2 mV	≤ 1.5 mV	≤ 400 μV
Geometrical noise (difference between channels for dark level)	≤ 2 mV	≤ 2 mV	≤ 2 mV	≤ 2 mV	≤ 100 mV
Non-linearity	≤ 2%	≤ 2%	≤ 2%	≤ 2%	≤ 1%
Electrical cross-talk	< 2%	< 3%	< 2%	< 2%	< –
Power dissipation	≤ 50 mW	≤ 50 mW	≤ 50 mW	≤ 100 mW	≤ 80 mW

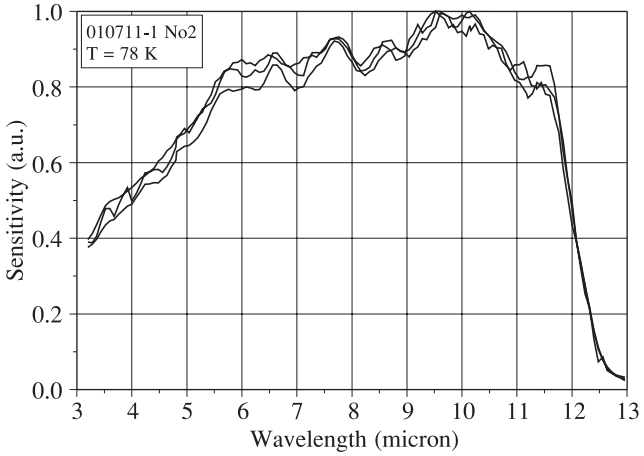

Fig. 7. Typical relative sensitivity of three photodiodes in one of the 4×288 modules.

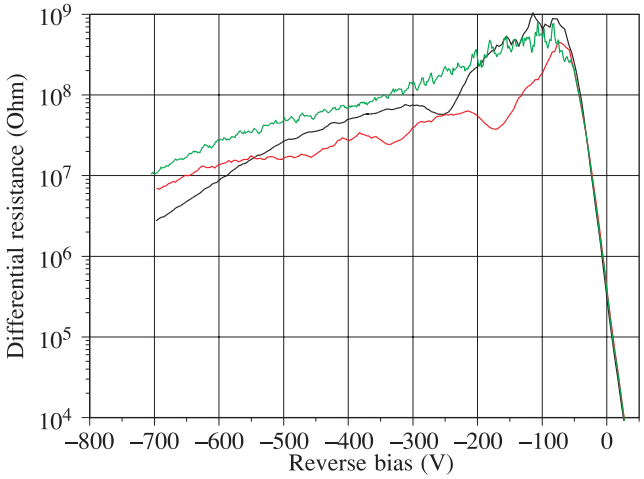

Fig. 8. Differential resistance of three photodiodes in different parts of 4×288 MCT array.

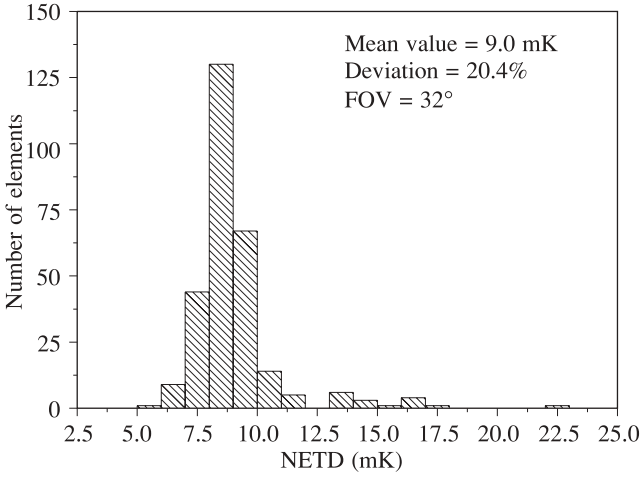

Fig. 9. NETD distribution in one of the 4×288 arrays.

pedances of the diodes to be in good coincidence with input ROICs transistors.

The NETD distribution is shown in Fig. 9. This parameter corresponds to the best parameters of matrix and MCT linear arrays with TDI function [3].

In Fig. 10, the sensitivity distribution along one of the linear arrays tested is shown. Switching on the deselection function to dead elements in the channels allows one to exclude the presence of dead elements or defective channels in the FPA.

Disconnection photodiodes control (deselection function) is accomplished by serial bi-phase register. The circuit for one bit of register includes the cell of shifting register, the cell of coefficient storage, and the cell of level converter. Using the voltage level of 3.5–5 V for deselection, one can exclude the level converter cell. All the cells are designed on the base of *D*-triggers, which have one information *D*-output and one synchronizing input. For control of a deselection register, three outputs are needed (additional outputs from cold zone), one output for information input, the second one for synchronizing output and memory loading input of deselection device. The total number of outputs is twenty two.

The sensitivity S_λ data were used for the detectivity D^*_λ evaluations according to the following expression [11]

$$D^*_\lambda = \frac{S_\lambda}{V_n} A^{1/2} \frac{1}{\sqrt{2\tau_{\text{int}}}},$$

where V_n is the noise level (in this case at the FPA output), A is the pixel area, and τ_{int} is the integration (accumulation) time. For any ROICs used, the mean detectivity obtained for all 4×288 FPAs with skimming mode included at T = 80 K, and background temperature T_b = 295 K, was in the range of $D^*_\lambda \cong (1.2–1.7)\times10^{11}$ cmHz$^{1/2}$/W for several arrays tested which almost corresponds to ultimate parameters possible. In Fig. 11, the detectivity distribution in one of the arrays tested is shown. The noise equivalent difference temperature for array with (CCD + CMOS) readout was *NEDT* ≈9 mK. For FPAs with other ROICs this parameter was of similar order. The dynamic range for arrays tested was within 67–77 dB.

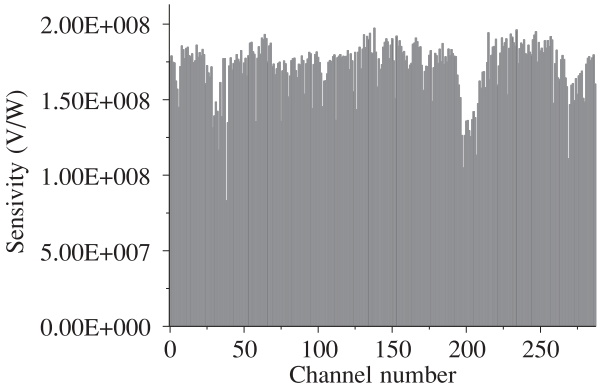

Fig. 10. Sensitivity distribution along 4×288 linear array with deselection function switch on.

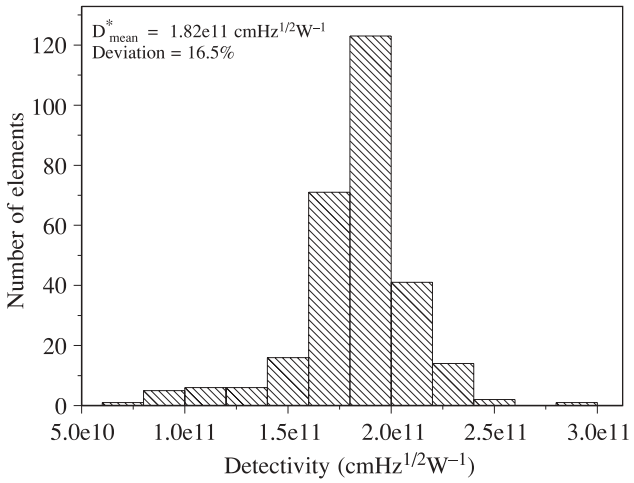

Fig. 11. Detectivity distribution in one of the 4×288 arrays.

Fig. 12. Thermovision imaging of a person by 4×288 FPA. Frame format 576×768.

Figure 12 shows thermovision imaging of a person obtained by 4×288 CMOS + CCD FPA with a frame format 576×768 (European format).

5. Conclusions

ROICs for linear arrays of different format were designed and manufactured. From the analyses executed of the ROICs known for 4×288 MCT arrays [2,3,12], it was concluded, that by basic parameters of ROICs mentioned above, they have similar parameters with known published data, though they were manufactured by different and not high level technologies. On their base ultimate performance of FPAs can be achieved. Further evolution of such kind of ROICs is possible only under the use of CMOS higher level technologies.

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