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Gate-controlled narrow band gap photodiodes passivated with RF sputtered dielectrics♣

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Gate-controlled diodes were made by using evaporated indium electrodes overlapping the edge of mesa diodes, isolated from the surface by a layer of ZnS or by native anodic oxide of InSb or HgCdTe. The resulting three-terminal device characteristics with gate voltage as a parameter have been investigated. Relative spectral responses and I–V characteristics were measured at 77 K. The R_0A product is used as an indicator of the dark current of photodiodes passivated with ZnS layer. A plot of R_0A values versus gate potential shows that the optimum R_0A values are obtained at small positive gate bias voltage. This dependence is consistent with surface recombination influencing the R_0A product. The results of a two-dimensional model for calculating gate-induce surface leakage currents due to band-to-band tunnelling are presented. The exact quantitative comparison cannot be made between our results and theory, since the active tunnelling area is not known.

Keywords: HgCdTe, InSb, photodiodes, passivation, sputtering

1. Introduction

Characteristics of semiconductor devices, in particular those made from narrow bandgap semiconductors, are to a large extent determined by the properties of the semiconductor surface and interfaces. The interface of semiconductor passivating layer plays important and often dominant role in determining device performance. Gate-controlled diodes are simple devices in analysis of surface passivation [1].

In a real p-n junction, particularly at low temperatures, an additional dark current related to the surface occurs. For the fabrication of high performance narrow band gap photodiodes, especially with small junction area, the surface passivation is essential. A method for determining the surface properties of semiconductor is investigated by C-V characteristic of MIS structures [2]. Band bending at the p-n junction surface can be controlled by a gate electrode overlaid around the junction perimeter on an insulating film. Several passivants have been used for photovoltaic devices, for example ZnS, CdTe, SiO_2, and natural oxides [3–5].

In this work a model analysing the influence of bulk and surface current contributions on the I-V characteristics for long-wavelength n^+–p HgCdTe photodiodes has been proposed. The effect of fixed insulator charge on the effective junction space-charge region is discussed. Carriers concentration, surface current, and R_0A product versus gate potential have been analysed. The results of calculation have been compared with experimental data.

2. Theoretical model of n^+–p junction

The quasi-two-dimensional model for calculation of gate-voltage induced surface leakage currents in n^+–p HgCdTe diodes is presented [6]. It is assumed that both the fixed charges in the passivant and the gate voltage are responsible for a negative surface potential, due to which the HgCdTe surface is accumulated. A schematic cross-sectional diagram of the n^+–p junction is shown in Fig. 1. The width of the depletion region on the p-side is pinched at the surface due to negative surface potential. The surface region is divided into sublayers of the thickness dx. The cur-

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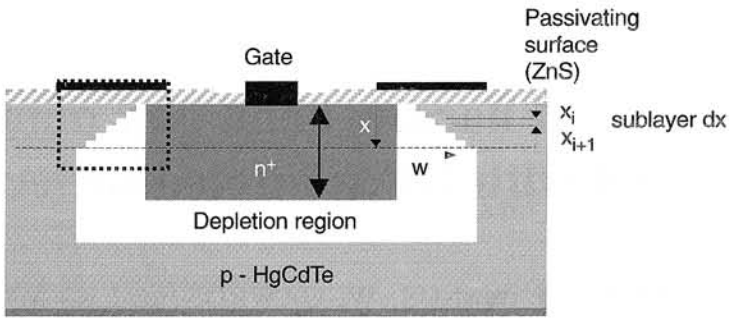


Fig. 1. Cross-sectional diagram of the HgCdTe diode.

rent contribution of each sublayer is evaluated by calculating the junction parameters as a function of the carrier concentration, which is different in each sublayer. All the current components are calculated in two dimensions, depth-wise (x) and laterally (w) as a function of depth, layer by layer, from the passivant--semiconductor interface (Fig.1).

The following assumptions have been made:

- the junction performance is dominated by the p-type side of the junction. This is usually the case when the n side is degenerated. The carrier concentrations N_D of the n^+ region is assumed as 1×10^{18} cm^{-3}. Thus the n^+-side depletion region is not taken into account;
- the effect of negative interface charges on n^+ region is neglected;
- the effect of fast interface states in the passivant is not incorporated, because their magnitude is appreciable only for non-zero bias;
- the acceptor dopant is fully ionised, so the equilibrium hole densities in the bulk $p_0 = N_A$;
- the minority carrier lifetime is determined by an Auger 7 mechanism.

Other assumptions will be further discussed.

The potential φ is defined as zero in the bulk of the semiconductor and φ_s (surface potential) at the semiconductor surface. The relations between the surface potential, space charge, and electric field can be obtained by using the one-dimensional Poisson equation [7]

$$\frac{d^2\varphi}{dx^2} = -\frac{1}{\varepsilon\varepsilon_o}\rho \tag{1}$$

where ρ is the total space-charge density given by

$$\rho = -q[n(x) - n_o] + q[p(x) - p_o] \tag{2}$$

Integrating Eq. (1) from the bulk to the surface and introducing the following abbreviations

$$F(\Psi,\gamma) = \sqrt{-[\gamma(1-e^{-\Psi}) + \frac{1}{\gamma}(1-e^{\Psi}) + \Psi(\frac{1}{\gamma}-\gamma)]}$$
$$\gamma = \frac{n_i}{p_o},\quad \Psi = \frac{e\varphi}{kT} \quad - \text{ the normalised potential,} \tag{3}$$

give the relation between the distance and potential

$$x(\Psi) = \int_{\Psi_s}^{\Psi} \frac{d\Psi}{F(\Psi,\gamma)} \tag{4}$$

The profile of the majority carrier concentration with depth in the surface layer is calculated from [7]

$$\Delta p(x) = p_{p0} L_D \int_{\Psi_s}^{\Psi(x)} \frac{e^{-\Psi} - 1}{F(\Psi,\gamma)} d\Psi \tag{5}$$

where $L_D = \sqrt{\varepsilon_0 \varepsilon_s kT/2q^2 n_i}$ – intrinsic Deby'e length.

We assume that the diffusion and band-to-band tunnelling mechanism dominate the diode's currents, and generation-recombination and trap-assisted tunneling currents are negligible [8].

The diffusion current density is [7]

$$J_{dif} = (qD_e n(x)/L_e)(e^{qV/kT} - 1) \tag{6}$$

where the minority carrier diffusion length and the diffusion coefficient D_e are given by the Einstein equation in terms of the mobility and the minority carrier lifetime associated with diffusion.

The band-to-band tunneling (btb) current density is obtained, as the electric field E function, assuming that particles having constant effective mass cross a triangular potential barrier, from [6]

$$J_{btb} = \frac{q^3 EV}{4\pi^2\hbar^2}\left(\frac{2m^*}{E_g}\right)^{1/2} \exp\left(\frac{-4\sqrt{2m^* E_g^3}}{3q\hbar E}\right) \tag{7}$$

where electric field is given as $E = (V_{bi} - V)/w$.

These current contributions are evaluated both in the bulk HgCdTe as well as in the surface layer separately in each sublayer. The total current and R_0A product are obtained numerically by calculation of the current in each sublayer, summation up the currents of all the sublayers, and then calculation of the resistance around the zero-bias point. Since the depletion width for an accumulated surface near the interface is pinched, the lateral area of the junction of each sublayer is also different. The lateral area has been approximated as in Ref. 5.

The expression for fixed charge densities due to the passivant Q_s, the gate voltage V_G, and the surface potential Ψ_s is given by

$$Q_s = V_G \frac{\varepsilon_0 \varepsilon_r}{d} = 2en_i L_D F(\Psi_s, \gamma) \tag{8}$$

where ε_r is the dielectric constant for passivated layer.

3. Experimental details

Two types of diodes have been investigated: planar HgCdTe and mesa InSb. The planar photodiodes were fabricated by ion milling of argon ions through the ZnS cap layer into p-type HgCdTe active layer. The starting material was p–type (10^{16} cm^{-3}) bulk $Hg_{0.78}Cd_{0.22}Te$ crystal due to cation vacancies with an n–type impurity background of 10^{15} cm^{-3}. Defined areas were then milled using a collimated, neutralised argon ion beam with energies of 0.5 keV with a current density of 3 A/m^2. The devices were further covered by protective layer of ZnS deposited at room temperature using RF magnetron sputtering system (as illustrated in Fig. 2). The contact to p-type region was made with alloyed Au on backside region. The contact to the n-type region and metal gate covering the p-n junction were prepared by indium evaporating.

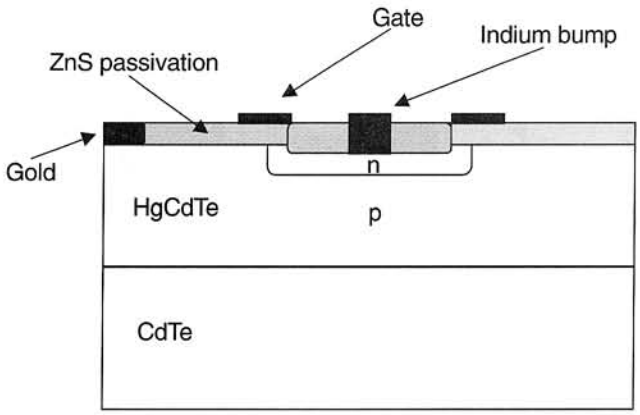


Fig. 2. Schematic draw of n^+-p HgCdTe gate photodiode.

The mesa InSb photodiodes were fabricated by Cd diffusion into n-type InSb active layer. The mesa structures were defined by standard photolithography techniques. The circular diodes of 300 μm diameter were fabricated by mesa etching to the n–region and passivated with anodic oxide. The anodization was made in standard 0.1 N KOH solution to prevent surface leakage. Vacuum evaporation of gold contacts was applied to the top of mesa. Electrical contact to the InSb substrate was made from indium.

4. Results and discussion

The exact profile of the majority carrier concentration p(x) as a function of depth (x) for various gate voltages is shown in Fig. 3(a). The depth of the accumulation layer (about 0.05 μm) is almost independent of U_g and is apparently a function of the substrate doping concentration N_A. The pinching of the p-side depletion region w as a function of depth is shown in Fig. 3(b). This depletion layer pinching causes a considerable increase in the electric field across the de-

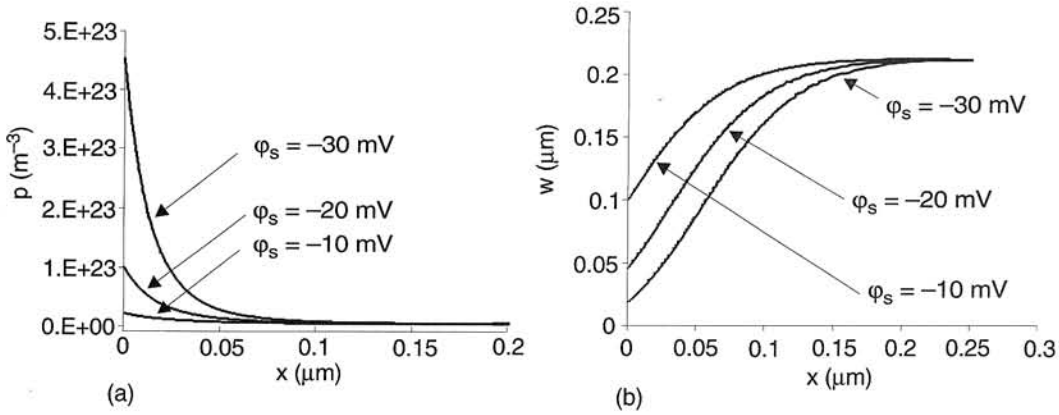


Fig. 3. Profile of the majority carrier concentration (a) and depletion region (b) as a function of depth for various surface potentials ($N_A = 5 \times 10^{15}$ cm^{-3}, x = 0.22, T = 77K).

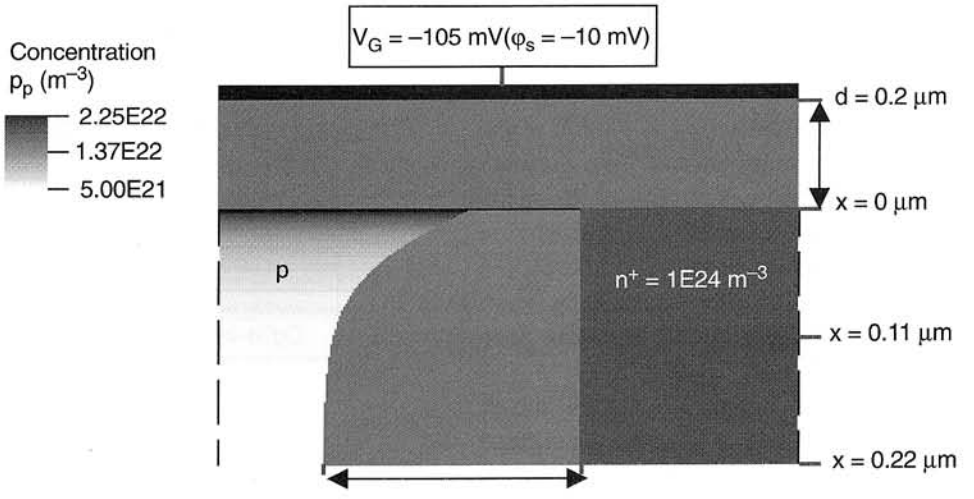


Fig. 4. Cross-sectional diagram of the n^+-p $Hg_{0.78}Cd_{0.22}Te$ junction near the passivant at 77 K.

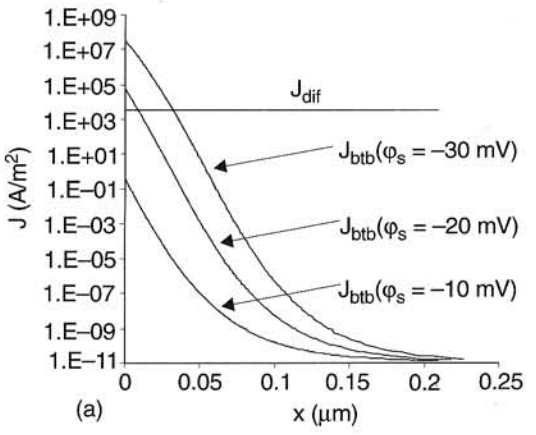
pletion region. As a result the btb tunnelling current increases drastically.

Cross-sectional diagram of the p-n junction near the passivant interface is shown in Fig. 4. It may be seen that the majority carrier concentration rises towards the surface. It also shows the pinching of the depletion layer, which increases as one approaches the interface.

The contributions from the different current mechanisms in terms of current density as a function of depth are shown in Fig. 5(a). The btb tunnelling current falls off sharply with depth, and dominates over the diffusion only close to the surface. The R_0A products, calculated for the different current mechanisms as a function of gate voltage, are shown in Fig. 5(b). According to Fig. 5(b) the net R_0A product is limited by surface btb tunnelling from the gate voltage higher then 0.1V (it corresponds to the surface charge density 2×10^{10} cm^{-2}). Thus, to avoid degradation of the R_0A by btb tunnelling, the value of interface charge density should be below this value.

The current-voltage characteristics of an InSb gate-controlled diode are given in Fig. 6. The characteristics exhibit the major effect of the surface potential upon the diode performance. At zero gate voltage the diode exhibits small excess curents in the reverse-bias region. Further increasing of the positive gate voltage increases the accumulation and leakage currents associated with the surface tunneling. The device exhibits negative differential resistance at $U_g > 4$ V. The passivation of InSb photodiodes is suitable.

The current-voltage characteristic of a HgCdTe photodiodes exhibits large excess current in the reverse bias region. Gate structure is required to separate surface and bulk effects. A plot of R_0A values versus gate potential shows that the optimum R_0A values are obtained at small positive gate bias voltage as shown in Fig. 7. At $U_g = 0$ accumulation is due to



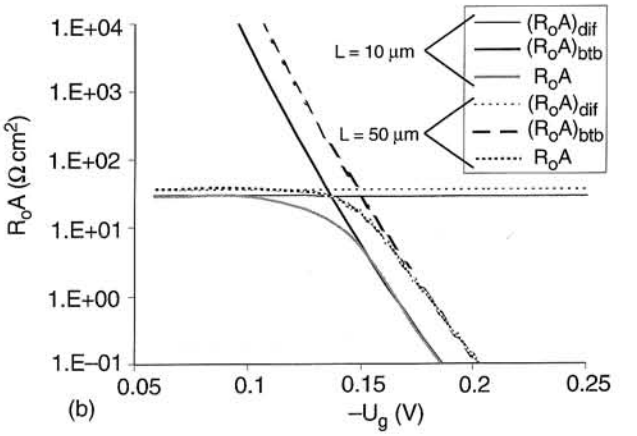


Fig. 5. Contributions from the different current mechanisms on current density (a) and R_0A product (b) ($N_A = 5 \times 10^{15}$ cm^{-3}, x = 0.22, T = 77 K).

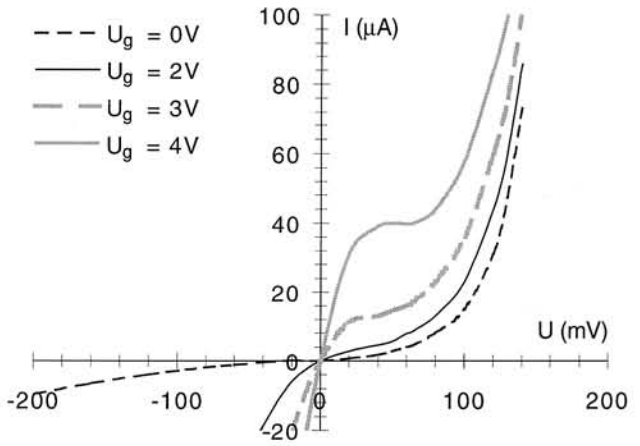


Fig. 6. Measurements of I–V characteristics for gate controlled InSb diode at 77 K.

the fixed interference charge density $Q_s = 5 \times 10^{10}$ cm^{-3}. The C-V measurements of MIS capacitors (In/ZnS/HgCdTe) are corresponding to gate-controlled diode experiment.

5. Conclusion

The effect of gate voltage on the surface accumulation layer has been accurately calculated and presented experimentally.

The main conclusions are:

- pinching of the depletion region significantly increases the electric field and lateral band-to--band tunneling current,
- acceptable fixed charge density may be calculated for gate voltage measurement,
- acceptable fixed charge density is a function of acceptor concentration and area of junction.

This method would also be applicable to other narrow-bandgap semiconductors after appropriate modifications.

From our results one can see that surface effects on performance of HgCdTe and InSb photodiodes are following:

- anodic oxide is a good pasivant of InSb diodes,
- RF sputtered ZnS layer induces high fixed charge density in HgCdTe photodiodes.

Acknowledgments

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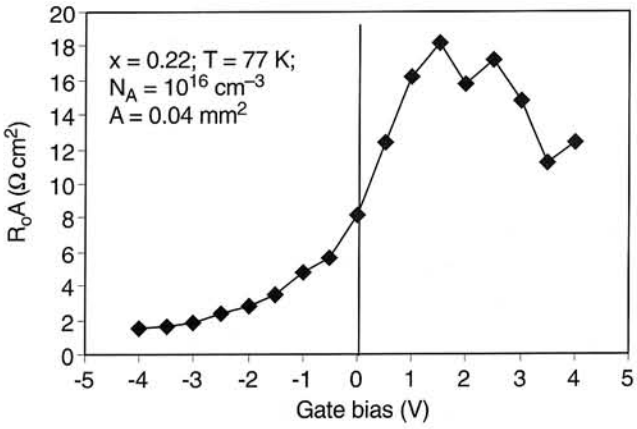

Fig. 7. Gate bias dependence of R_0A for n^+-p HgCdTe photodiode.

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