Invited paper

OPTO-ELECTRONICS REVIEW 7(4), 259–269 (1999)

Low-noise infrared and visible focal plane arrays

L.J. KOZLOWSKI[1*], K. VURAL[1], J. LUO[1], A. TOMASINI[1], T. LIU[2], and W.E. KLEINHANS[2]

[1]Rockwell Science Center, 1049 Camino dos Rios, Thousand Oaks, CA 91360, USA
[2]Valley Oak Semiconductor, 31255 Cedar Valley Drive Suite 314 Westlake Village, CA 91362, USA

While charge-coupled device (CCD) technology is often perceived to provide nearly optimum signal multiplexing and very low imager noise, coupling high performance detectors (at cutoff wavelengths from 0.6 μm to 17 μm) to CMOS multiplexers provides lower (< 10 e⁻) read noise at high data rates using several pixel amplifier schemes. This superiority is fundamental and has been validated on infrared and visible focal plane arrays. Thus the robust pixel-based signal amplification facilitated by sub-micron CMOS is stimulating low-noise focal plane array (FPA) development for discriminating applications including infrared astronomy, wavefront sensing, spectroscopy, and spaceborne imagers. Enabled by Moore's Law and concomitant increases in integration density, commercial imagers for consumer video are also providing very low read noise and high sensitivity. Hence we report the ability to usefully detect quanta at non-cryogenic operating temperatures because read noise is at the single-electron level at high video rates. While such advances are typically first demonstrated on infrared sensors, the enhancements migrate to visible devices as soon as the available lithography of the prevailing silicon CMOS technology permits, because visible imager pixels are necessarily much smaller to match the optical blur.

Keywords: FPA, infrared, CMOS, CCD, MWIR, LWIR, low-noise.

1. Introduction

Recent advances in detector materials and CMOS processes are resulting in the rapid proliferation of infrared sensor products [1]. Full-featured, high-resolution products are now widely available in many formats. Figure 1 summarizes FPA availability versus FPA pixels and operating wavelength. SWIR (up to 2.5 μm) and MWIR (up to 5.5 μm) FPAs now have pixel counts previously available only with visible CCDs. Visible imagers are migrating to film-type resolution.

This natural evolution follows from the ongoing maturation of high-performance detector materials [2], the chronic proliferation of detectors including the emergence of uncooled sensors and alternative cooled materials, and the exploitation of commercial CMOS for developing increasingly sophisticated readouts. The world's first high-performance 1024×1024 IRFPA was developed in mid-1994 for infrared astronomy (0.8 to 2.5 μm) with about 3.2 million transistors, for example [3]. In early 1995 [4], a more sophisticated 1024^2 FPA with 4.3 million transistors was subsequently developed for sensing radiation to 3.2 μm wavelength at 120 K. In late 1997, a multi-mission 1024×1024 FPA was developed that senses radiation to beyond 10 μm. Its CMOS readout

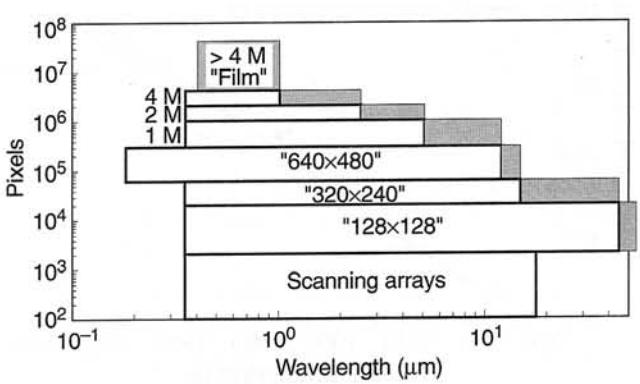

Fig. 1. Visible and infrared focal plane array formats currently available and in development.

*e-mail: ljkozlow@rsc.rockwell.com

uses 0.5 μm technology, has ~ 7.5 million transistors and provides multi-mode operation because of its order-of-magnitude higher functionality. The 2048× 2048 FPA now being developed for infrared astronomy has 13,059,900 transistors [5]. These and other readouts for infrared FPAs have about the same number of transistors as integrated in contemporary microprocessors at each moment in time. An important distinction is that the majority of transistors in the infrared readouts perform low-noise analog functions rather than logic, memory or computing.

Figure 2 compares the chronology of advanced integrated circuit development for leading microprocessors (for personal computers and engineering workstations) and infrared focal plane arrays produced by Rockwell Science Center of Thousand Oaks, CA. Contemporary CMOS readouts clearly use as many transistors as the latest microprocessors.

Though many visible FPAs use CCD technology for low-noise image capture, pixel-based amplification via CMOS fundamentally provides performance advantages with respect to temporal noise and electrical sensitivity. The minimum theoretical read noise of a CCD is limited in large format imagers by the output amplifier's thermal noise after correlated double sampling (CDS) is applied in off-chip support circuits. The alternative CMOS paradigm offers lower temporal noise because the relevant noise bandwidth is fundamentally several orders of magnitude smaller and better matches the signal bandwidth. While CCD sensitivity is constrained by the limited design space involving the sense node and the output buffer, CMOS sensitivity is limited only by the desired dynamic range and operating voltage. CMOS-based imagers also offer practical advantages with respect

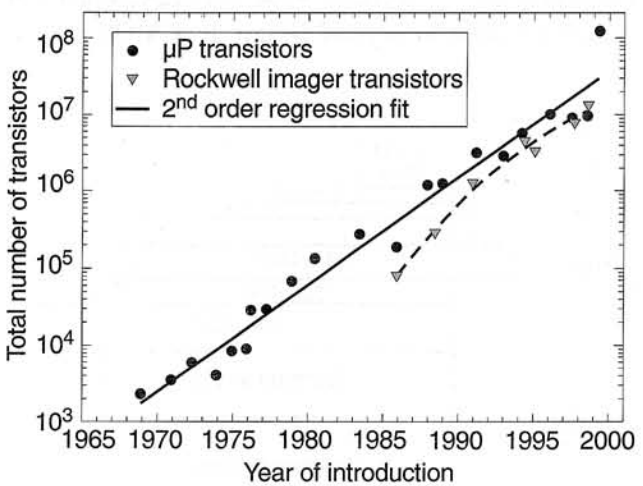

Fig. 2. Chronology of transistor count for advanced integrated circuits.

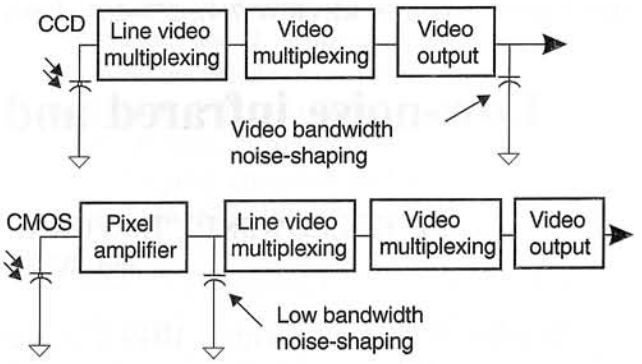

Fig. 3. The CMOS paradigm with pixel-based amplification (e.g. CTIA) and noise bandlimiting.

to on-chip integration of camera functions including command and control electronics, digitization and image processing.

Figure 3 compares the typical CCD and CMOS architectures wherein CMOS pixel amplifiers support relatively low line rates rather than the full video rate as in a CCD. The requisite band-limiting, facilitated on-chip, corresponds to much lower noise bandwidth than in the CCD paradigm. Because the pixel-based amplification also minimises vulnerability to EMI within the imager, the output buffer's wideband noise is rendered negligible, essentially independent of the actual video rate.

A second advantage is the relative ease at which higher sensitivity is achieved in the CMOS imager paradigm. A small feedback capacitance is easier to implement in a CMOS-based capacitive transimpedance amplifier, for example, because the analog capacitor serves no other function so that it can be optimally designed and fabricated. Though each pixel's amplifier clearly increases the pixel-to-pixel fixed pattern noise relative to the single-output CCD model, many high performance sensors employ full-frame memory to compensate various such nonuniformities, including aperture shading.

Hybrid infrared FPAs have used CMOS readouts since ~ 1985 for low-noise readout of photo-generated signals. Shrinking circuit geometries and advances in imager design have since enabled rapid improvements in the performance of the CMOS readouts used for infrared detector interface. CMOS with minimum feature ≤ 0.5 μm is also enabling monolithic visible CMOS imagers, because the denser photolithography allows low-noise signal extraction and high performance detection with high optical fill factor within each pixel. This "sudden" emergence of CMOS imagers for sensing visible light is, hence, only one more consequence of Moore's Law, which

predicts a doubling of transistors for each integrated circuit about every 18 months.

2. CCD architecture

Charge coupled device technology is very mature with respect to fabrication yield and attainment of near-theoretical sensitivity. In a CCD, the photogenerated carriers are first integrated in the well formed by a photogate and subsequently transferred to slow and fast CCD shift registers. The charge is then converted to a voltage at a sense node often formed by a floating diffusion typically having 6 to 12 fF capacitance. Both the photovoltage and the floating diffusion's reset voltage are serially read to form standard rasterized video after straightforward suppression of the sense node's reset noise and the output buffer's 1/f noise via off-chip CDS. The dominant sources of read noise after CDS include the wideband noise of the output amplifier and, possibly, excess noise of the video electronics. Both are minimised by reducing the sense node capacitance and, hence, maximizing the conversion gain. Various schemes can minimize sense capacitance, including two-stage amplifiers and alternative readout node designs, but the requirement to drive the video signal at ten to one hundred MHz limits the efficacy of these schemes.

Practical considerations for sense node capacitance, video dynamic range, output amplifier bandwidth, and excess noise in the camera electronics suggest a conventional noise analysis to estimate the read noise depending upon the number of imager pixels, the camera frame rate and several key design assumptions. The minimum video rate assuming single output tap is approximately

$$f_{video} = 2 \times \text{Rows} \times \text{Columns} \times f_{frame} \qquad (1)$$

where the prefactor 2 accommodates the fact that both the signal and reset level are read from a CCD to facilitate CDS. The video from CMOS imagers typically comprises only the pixel signals and not the reset levels.

We assume that an appropriately sized on-chip amplifier is used to drive a 50 pF load with 1 V signal swing. We also assume minimum source follower gain of 0.9, 6 fF or 12 fF sense capacitance, 30 Hz frame rate, and an output bandwidth compatible with ten time constants of settling at each respective video data rate. Without off-chip correlated double sampling, the predicted read noise at C_{sense} of 12 fF is

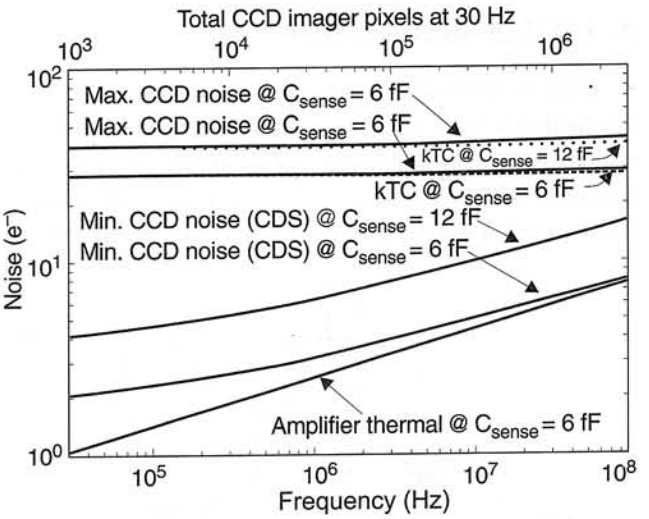

Fig. 4. Theoretical CCD read noise vs. video frequency.

about 40 e^- regardless of array size, but reduces to about 28 e^- at C_{sense} of 6 fF. By applying CDS, the read noise is reduced in both cases by suppressing kTC noise. The predominant noise source becomes the output amplifier's thermal noise (N_{amp}). For an array comprising 1.3 million pixels, for example, the minimum CCD read noise at 40 MHz data rate reduces to about 14 e^- and 7 e^- at 12 fF and 6 fF, respectively. Figure 4 plots the estimated CCD noise vs. video frequency. While 1 e^- read noise is theoretically possible at 20 kHz data rate if the CCD noise is the predominant camera noise, the more likely noise level for a video CCD operating at 20 MHz is 10 to 20 e^-.

While further reduction in sense node capacitance is in principle possible, practical considerations instead mandate reducing the frame rate to minimize the input-referred read noise as suggested by this analysis. Astronomy CCDs, for example, are typically operated at about 10 kHz data rate to appropriately constrain the output bandwidth to enable reaching the single electron noise level. Such band-limiting limits the output amplifier's thermal noise, the Johnson noise of the load resistor and excess camera noise. However, this approach suggests that a single-output one megapixel CCD would have to operate at 0.1 Hz frame rate. Since long exposures are often needed for astronomy, such low frame rates and long readout times are not problematic in this case. Most other applications involving human gratification, such as video and digital image capture, are not so forgiving in this respect. Adding output taps moves the CCD to the CMOS paradigm where such amplification is more readily facilitated without adversely increasing nonuniformity or power dissipation.

3. CMOS architecture

CMOS-based imagers for both infrared and visible applications use either active or passive pixels, as shown in simplified form in Fig. 5 [6]. Active-pixel sensors (APS) exploit some form of amplification at each pixel. Passive pixels are instead read without in some cases, creates artifacts in the imagery by generating electrical currents in the active circuitry.

Active pixel sensors incorporate transistors in each pixel to convert the photo-generated charge to a voltage, amplify the signal voltage and reduce noise. Adding these components reduces the fill factor of monolithic imagers to about 30 to 50 percent in

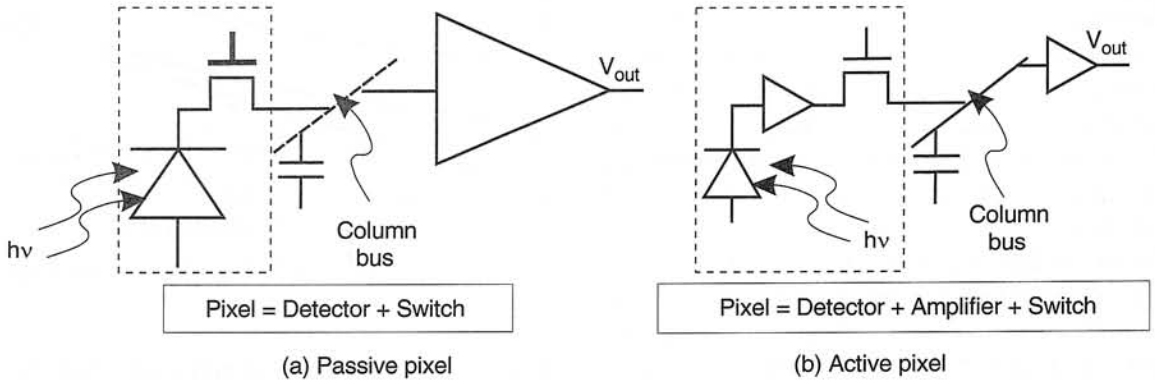

Fig. 5. Passive and active pixel sensors.

pixel-based amplification. Since passive pixel sensors (PPS) have simple pixels consisting of as few as two components (a photodiode and a MOSFET switch), circuit overhead is low and the optical collection efficiency (fill factor) is high, even for monolithic devices. The large optical fill factor of up to 80% maximises signal collection and minimizes fabrication cost by obviating the need for microlenses. Microlenses are a standard feature of CCD and CMOS APS imagers for visible applications. When accurately deposited over each pixel, microlenses concentrate the incoming light into the photosensitive region (Fig. 6). When the fill factor is low and microlens arrays are not used, the light falling elsewhere is either lost or, 0.5 μm processes at 5 to 6 μm pixel pitch or in 0.25 μm processes at 3.3 to 4.0 μm pixel pitch.

A very efficient scheme for simultaneously maximizing optical fill factor and the available pixel real estate is the vertical hybrid approach. In this type of multi-chip module, which is the predominant methodology for infrared FPAs, the signal detection and readout functions are segregated via flip-chip hybridization. Figure 7 shows the typical hybrid solution for infrared FPAs: the IR detection is performed in a detector array specifically optimized for the desired spectral band, the low-noise readout is performed in a CMOS-based readout, and the mechanical and electrical interface is facilitated via indium interconnects.

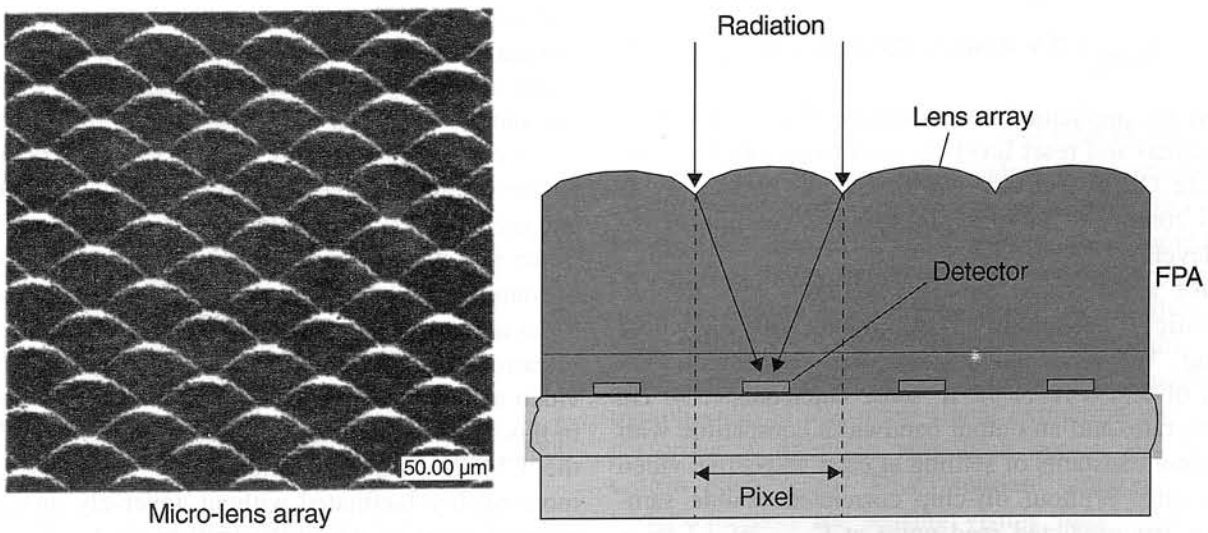

Fig. 6. Micrograph and cross-sectional drawing of microlensed hybrid focal plane array.

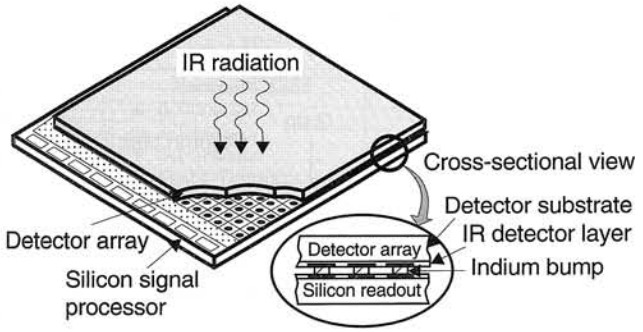

Fig. 7. Hybrid FPA with independently optimised signal detection and readout.

Hybrid manufacture allows the CMOS readout to be fully optimized to the extent that the available process allows. Figure 8 shows the block diagram for a typical CMOS multiplexer with CTIA input. In this case the sense capacitance, as defined by the feedback capacitor, C_{fb}, can be made significantly smaller than 10 fF. Figure 9 plots as-drawn feedback capacitance versus measured FPA conversion gain. Feedback capacitance as small as ~ 1.7 fF has been achieved for applications requiring high electro-optical sensitivity. In contrast to the broad range already achieved in CMOS-based imagers, the CCD provides limited sensitivity and sensitivity range.

The schematic for the basic capacitive transimpedance amplifier is shown in Fig. 10 along with alternative low-noise designs, including the source follower per detector and gate modulation with MOSFET load. Johnson provides a clear foundation for some of the well-known and practical rules that apply to sensor amplifiers in use today including these schemes [7]. In the CTIA, the kTC noise normally generated by resetting the detector is suppressed via negative feedback. However, a bandwidth-

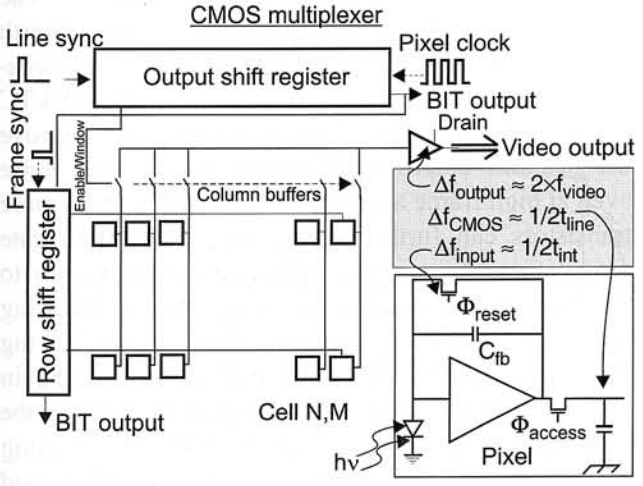

Fig. 8. CMOS multiplexing readout with CTIA detector interface.

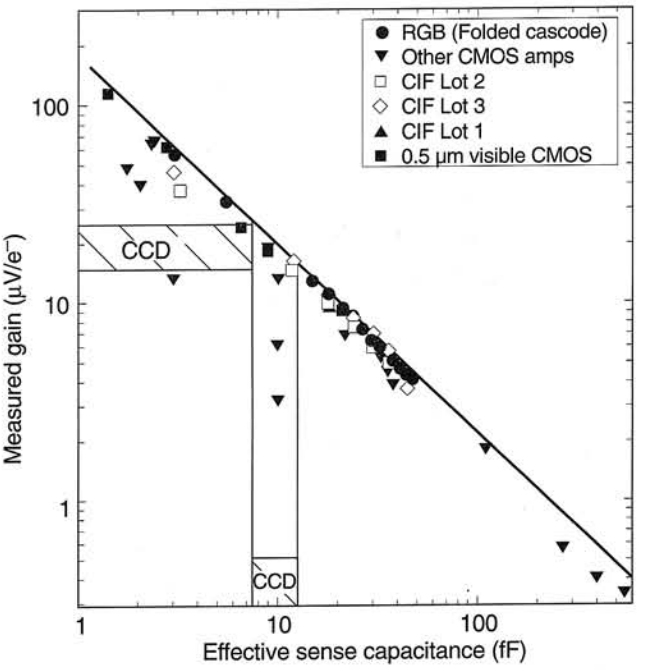

Fig. 9. As-drawn feedback capacitance vs measured gain.

-dependent noise remains which is proportional to the feedback capacitance and inversely proportional to the band-limiting capacitance. The closed-loop gain degradation caused by input capacitance boosts the high frequency noise proportional to the composite input capacitance formed by the parallel combination of the detector (plus input stray) and feedback capacitance. The high frequency noise, however, can be mitigated via appropriate bandlimiting depending on the necessary line rate. The resulting white noise in electrons is approximately

$$N_{channel} = \sqrt{\frac{nkTC_{fb}}{q^2} \frac{(C_{det} + C_{fb})^2}{C_L(C_{fb} + C_{det}) + C_{fb} + C_{det}}}, \quad (2)$$

where the prefactor n is one or two depending on single-ended or differential amplification, respectively. C_{fb} is the feedback capacitance including the Miller capacitance and integration capacitance, C_{det} is the detector capacitance, and C_L is the load capacitance. The CTIA's load capacitor can suppress the wideband "channel" noise depending on the signal bandwidth needed to support the line rate. Similar bandwidth optimisation and noise reduction is available in the various other CMOS circuits used for detector interface.

Source follower read noise, for example, ranges from the reset noise associated with resetting the detector, to as low as the post-CDS value previously described [8]. The post-CDS read noise is expressed

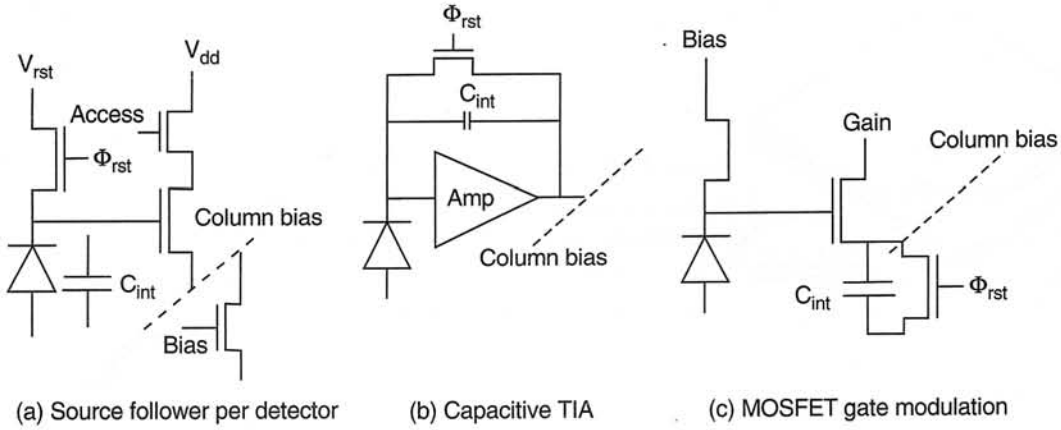

Fig. 10. Low noise APS circuits for hybrid and monolithic focal plane arrays.

$$N_{Post-CDS}(e^-) = \frac{2^{1/2}}{S_v}\sqrt{\int_0^{f_{max}} V_n^2(f)\left[\frac{1-\cos 2\pi f t_{C-S}}{1+(p f t_{C-S})^2}\right]df} \qquad (3)$$

where $V_n(f)$ is the MOSFET noise spectral density as a function of frequency, t_{C-S} is the CDS time constant set by the read process and S_v is the readout conversion gain in V/e$^-$. As with the CTIA, the noise bandwidth is tuned for the maximum required signal bandwidth. Since the amplifier operates at the line rate, the requisite bandwidth is orders of magnitude lower than for a CCD. The electrical sensitivity, as denoted by S_v, is optimised independent of bandwidth considerations.

Figure 11 shows both the resulting theoretical and empirical noise performance for both the CTIA and SFD versus input capacitance. Included are various infrared and visible focal plane arrays with detector capacitance spanning about two orders of magnitude. To directly compare with CCD imagers at equivalent pitch, detector capacitance below ~ 10^{-13} pF is relevant. Here the read noise is generally below ~ 30 e$^-$ and as low as 3 e$^-$, even though the various frame rates are video rate or higher and the video rates range from to 2 to 40 MHz.

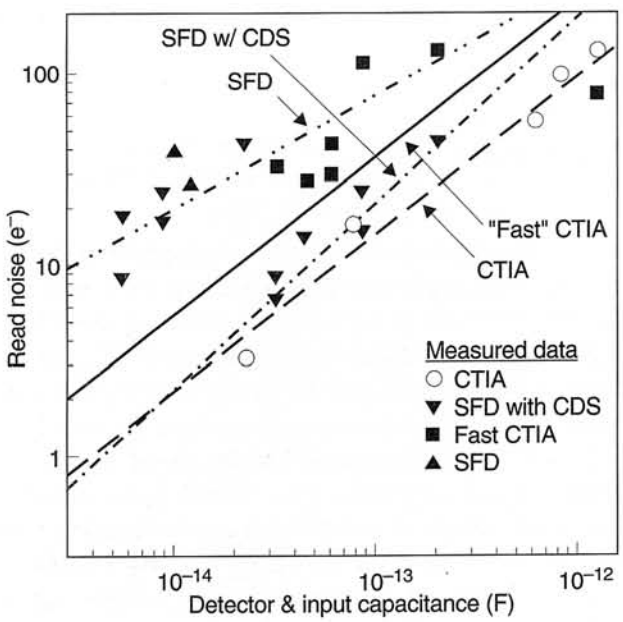

Fig. 11. FPA read noise vs. capacitance for CTIA and SFD implementations.

Of highest relevance for direct comparison with CCDs are the read noise levels for capacitance 30 fF. The data obtained without invoking correlated double sampling are in excellent agreement with the expected values for this kTC-limited scenario. The other data points for the SFD with CDS and the CTIA also agree with theory and surpass those achievable with a scientific CCD at video data rates.

The SFD basically uses three transistors to transduce the photo-generated signal. The first and second transistors in the pixel provide pixel access and reset. The third facilitates current amplification in conjunction with a current source outside of the pixel. The CTIA, on the other hand, essentially adds a fourth transistor to provide voltage amplification and negative feedback in the pixel to minimize the net kTC noise. Integrating additional transistors can improve the detector amplifier to further reduce read noise even at high frame and video rates. Adding even more transistors can further reduce the noise. With gate modulation, for example, adding a fifth transistor to the pixel provides gain in the charge domain by using a load MOSFET to modulate the current flowing through a gain MOSFET. The resulting front-end gain mitigates the kTC noise generated upon resetting the integration capacitance. Figure 12 shows the resulting performance gains as evidenced by the lower read noise achieved with the "five transistor" amplifier, in-

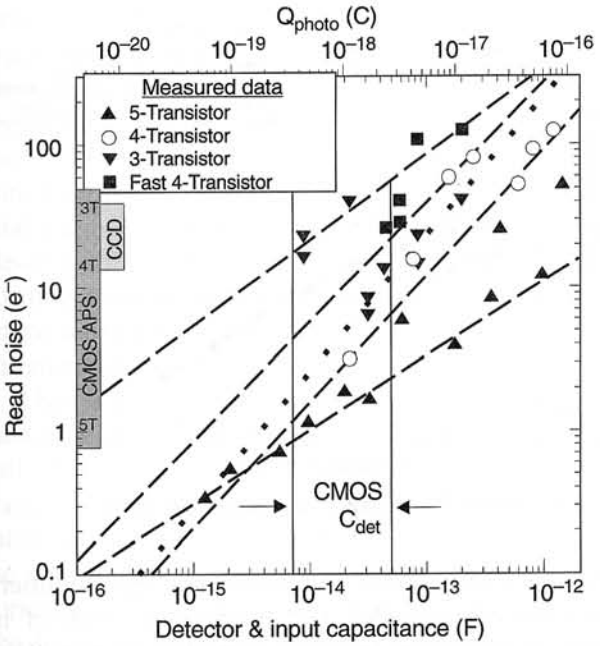

Fig. 12. Read noise vs capacitance for three, four, and five transistor CMOS detector interface circuits.

cluding average noise less than one electron. While this feature has already allowed gate modulated FPAs to yield sub-electron read noise, further reduction in detector capacitance and amplifier bandwidth are needed to enable the source follower and CTIA to do likewise.

Adding several transistors to gate modulation enables a circuit variant called buffered gate modulation (BGM). The additional MOSFETs reduce image lag and improve all performance aspects so that high performance low-light-level imaging is now possible.

4. Focal plane array validation

These and other low-noise APS schemes have been integrated into various focal plane arrays. In this section we succinctly report the measured performance characteristics of several key devices. Figure 13 plots the peak detectivity (D*) versus operating temperature for these and prior demonstration FPAs. Also plotted are the theoretical limits vs temperature for 1.5 μm, 2.5 μm, and 3.4 μm photovoltaic detectors. The D* reaches the background-limited plateau as the temperature is lowered for each specific test condition, except for the most recent buffered gate modulation FPA data at extremely low background (1.7 μm HgCdTe/BGM at 2×10^3 photons/cm^2s background). In this case our preliminary data suggest that this low-noise FPA may be operating at a limit governed by the D*f* product and the MOSFET 1/f noise, where f* is the intrinsic D* bandwidth for the circuit. Lengthening the integration time to increase the signal integrated during the integration epoch also increases the integrated 1/f noise and thus

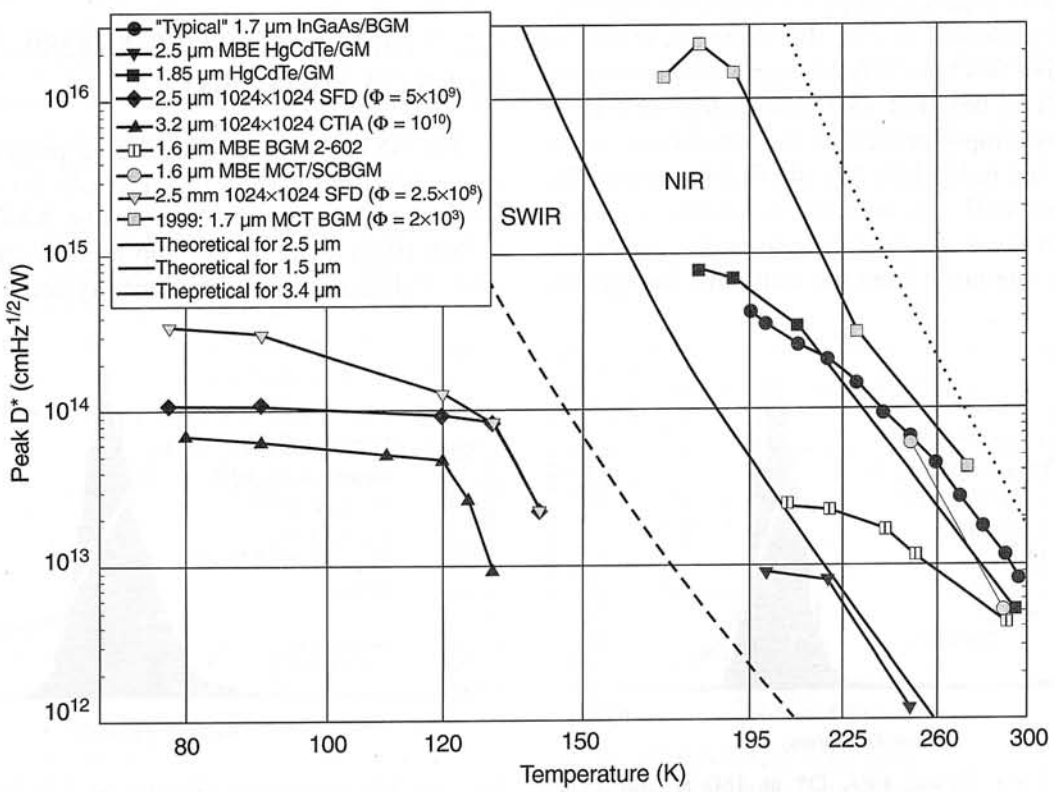

Fig. 13. Peak D* of low-noise near-infrared and SWIR FPAs at low background.

lowers the D*. Alternatively shortening the integration time decreases the integrated signal, thus implying insufficient signal bandwidth, thereby lowering the D*. Additional data are needed to determine the empirical D*f* product. Nevertheless, the maximum attained D* is extremely high at 2.4×10^{16} cmHz$^{1/2}$W^{-1} (Jones).

4.1. Infrared gate modulation: 1.7 μm 128×128

The TCM1717 is a 128×128 with 60 μm pixel pitch. Each pixel comprises an advanced gate modulation circuit in 0.8 μm CMOS. Mean read noise < 1 e$^-$ was measured at up 5 MHz data rate (250 Hz frame rate) for both near-infrared (NIR) and visible hybrid FPAs. A near-infrared (NIR; 1.7 μm) hybrid IR FPA has yielded D* exceeding 2×10^{16} Jones at 180 K (Fig. 14). A visible hybrid fabricated with silicon p-i-n detectors has similarly yielded ~ 1 e$^-$ read noise at about 250 K. The device is sufficiently sensitive to detect self-emission of hot carriers along the FPA sides, where the digital shift registers and the output amplifier resides.

While the various measurements at the extremely low operating background of 2×10^3 photons/cm^{2}s strongly suggest that the FPA may be operating at a near-term practical limit governed by the device's practical D*f* product and its 1/f noise, the measured D* is unprecedented at 2.4×10^{16} Jones. It is not yet clear whether this limit is fundamental for this type of amplifier (i.e., buffered gate modulation) or can be obviated by simply enhancing the amplifier's maximum gain and bandwidth. We did find that increasing the background flux to increase the amplifier's bandwidth under these stressing conditions also lowers the D* via the shot noise from the additional background flux. We also found that increasing the amplifier's bias current degraded D*, likely as a result of increased hot carrier luminescence (data labeled "High I_{amp}"). These data are plotted in Fig. 15 where D* is shown vs integration time at two backgrounds. Significantly increasing the operating temperature caused the D* to be detector-limited, as expected. Figure 16 is a D* histogram at 230 K operating temperature and 2×10^8 photons/cm^{2}s background where the mean value is 4.2×10^{13} Jones. This is the best yet achieved with a NIR (1.7 μm) FPA at this temperature, which is compatible with two-stage thermo-electric coolers.

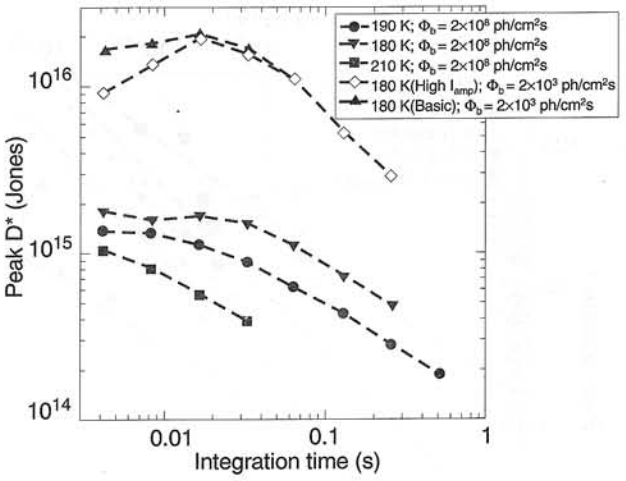

Fig. 15. NIR FPA Peak D* vs integration time.

4.2. Visible CMOS SXGA (1280×1024) and XGA (1024×768)

The SXGA CMOS imager is a progressive scan (non-interlaced) CMOS image sensor for single-chip still or video cameras requiring SXGA format (1280×1024) at frame rates up to 30 frames per second. Fabricated in Conexant Systems (Newport

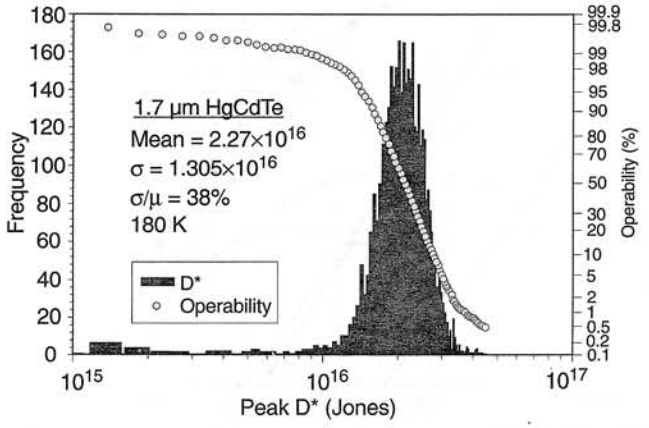

Fig. 14. 1.7 μm hybrid FPA D* at 180 K and 2×10^3 photons/cm^{2}s background.

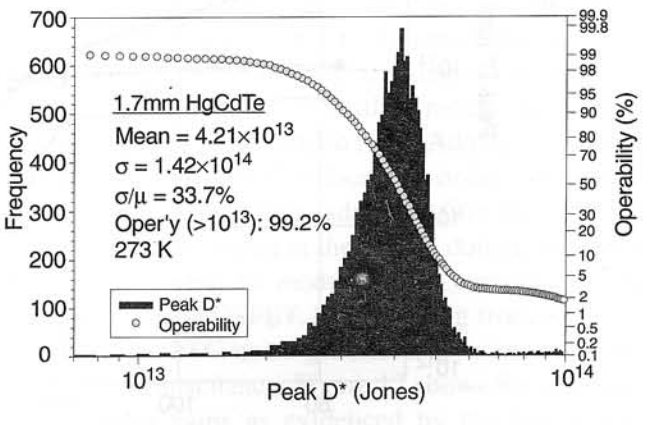

Fig. 16. 1.7 μm hybrid FPA D* at 230 K and 2×10^8 photons/cm^{2}s background.

Beach, CA) 0.5 μm analog CMOS process, the active image-sensing area is configured as 1024 horizontal lines, each having 1280 elements per line. The image-sensing area is bordered on all four sides with four rows/columns of black pixels (on the right side with three black columns and one white column). The total number of pixels is therefore 1288 by 1032. Single-chip colour-sensing capability is achieved by depositing a colour filter matrix and microlenses on the image-sensing area. This matrix is not used for monochromatic devices.

The XGA imager is a progressive scan (non-interlaced) CMOS image sensor for single-chip still or video cameras requiring XGA format for frame rates up to 24 frames per second. Also fabricated in Conexant's 0.5 μm analogue CMOS process, the active image-sensing area is configured as 768 horizontal lines each having 1024 elements per line. The image-sensing area is bordered on all four sides with four rows/columns of black pixels (on the right side with three black columns and one white column). The total number of pixels is therefore 1032 by 776. Single-chip colour-sensing capability is achieved by depositing a colour filter matrix and microlenses on the image-sensing area. This matrix is not used for monochromatic devices.

The active pixel circuitry in each of these devices consists of a diode in which the incoming photons are converted to electrons and an amplifier. During the integration time, all the generated electrons are stored on the diode junction capacitance. At the end of the integration time, the analogue pixel voltage is transferred to the column wire through the pixel amplifier, where the column buffer further amplifies the voltage when necessary.

The key difference between the SXGA and XGA-2 is the manner in which the pixels are reset after readout. The SXGA is reset in a relatively conventional fashion – kTC noise suppression is subsequently handled in the column buffer. The XGA, on the other hand, uses a patent-pending reset scheme to suppress the kTC noise at the pixel without having to invoke correlated double sampling and thus require full frame memory.

The video gain in both devices is adjusted by three control bits. The column buffer also performs signal processing to reduce temporal and spatial noise. The basic SXGA conversion gain (mode 000) is about 32 μV/e⁻, which is 60% higher than a typical astronomy CCD and about 100% higher than a typical video CCD. Higher gains include a "2X" mode 61 μV/e⁻ (mode 001), a "4X" mode that yields 110 μV/e⁻ (mode 010), and several other modes through "8X". The highest SXGA gain setting yields 440 μV/e⁻ gain for low-light level imaging with roughly 8 bit dynamic range.

The basic sensitivity for the XGA-format CMOS imager is 18 μV/e⁻. This is lower than the SXGA, because the photodiode is significantly larger (7 μm pitch vs 5.6 μm pitch). This device has sixteen possible gains with the highest at ~ 250 μV/e⁻ and the lowest at 18 μV/e⁻.

In the basic gain mode, the SXGA has an operating range of 1.2 V with a 600 μV noise floor for a dynamic range of 66 dB. The fixed pattern noise floor is lower than the temporal floor, at 360 μV. Relative to the maximum signal, the fixed pattern noise is less than 0.04% and can be further reduced off-chip by simply providing an offset term for each column of the imager. The other gain modes have larger operating range of 1.8 V. The XGA imager has smaller operating range of 0.9 V, but its 300 μV noise floor translates to nearly 70 dB dynamic range.

CMOS imager read noise was measured using a standard characterisation apparatus comprising a 14-b and a 12-b A/D converter and a Preamble Model 1855 preamplifier with programmable bandwidth as large as 100 MHz. The SXGA's rise and fall times of 3.5 ns and 7 ns, respectively, allowed settled video signals to video rates 40 MHz. Minimisation of output amplifier ringing required careful chip interface to minimise lead inductance. Preliminary tests performed on a subsequent version of the XGA with on-chip 10b A/D converter indicate, as expected, that the technical challenges posed by this analogue interface are greatly eased by migrating the converter to the imager die.

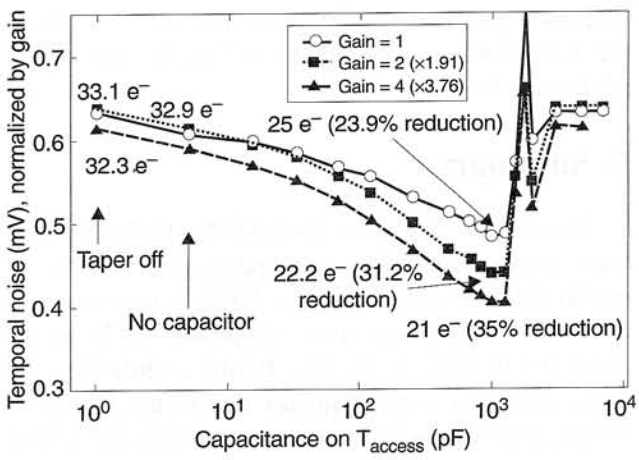

Fig. 17. CMOS XGA read noise vs. gain and external waveform conditioning capacitance.

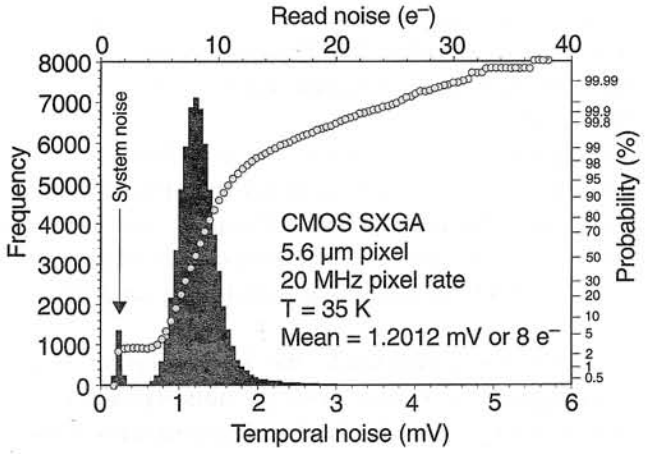

Fig. 18. CMOS SXGA read noise at "4X" gain.

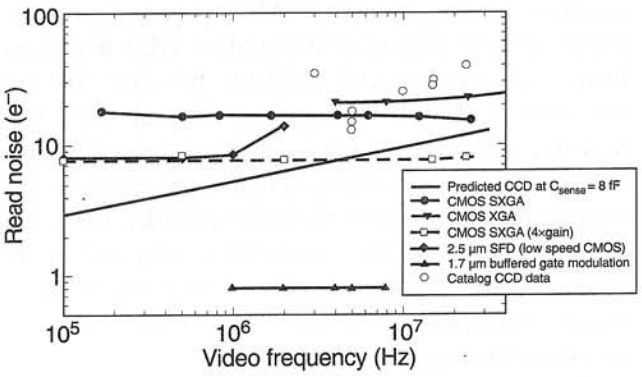

Fig. 19. Read noise vs. video frequency for CCD and CMOS imagers.

Figure 17 shows the measured CMOS XGA noise vs. signal for basic gain (18 µV/e⁻), "2X" gain (34.4 µV/e⁻) and "4X" gain (67.7 µV/e⁻). The minimum read noise with optimum external waveform conditioning capacitance of ~1 nF drops slightly from about 25 e⁻ to about 21 e⁻ at the highest gain. While the kTC noise for the 8.9 fF detector capacitance normally translates to a read noise of about 33 e⁻, the on-chip kTC noise suppression circuit reduces this fundamental noise level by 180% without invoking correlated double sampling.

This demonstration of kTC noise reduction without the use of correlated double sampling and the concomitant need for off-chip memory to store each pixel's reset level for intraframe subtraction suggests many other future signal processing enhancements in the CMOS paradigm.

The SXGA imager has nominal detector capacitance of ~5 fF. As expected, hence this device yielded lower read noise than the XGA. At the "4X" gain setting corresponding to conversion factor of 130 µV/e⁻, the 1.2 mV mean noise shown in Fig. 18 translates to read noise less than 10 e⁻.

5. Summary

Figure 19 summarises the SXGA and the XGA results along with CCD data gathered from various manufacturer catalogues. The XGA's read noise of about 21 e⁻ is lower than competing CCD imager noise at ~10 MHz video rate. Further, while the CCD noise increases with frequency due to the increasing output amplifier white noise as expected, the CMOS data is essentially independent of bandwidth because the dominant noise mechanisms do not depend on the video rate and associated bandwidth. This advantage increases with the number of pixels. The larger format, smaller pixel and higher sensitivity SXGA imager is thus superior to the competing CCDs at a lower video frequency of ~5 MHz. In the basic operating mode used for digital still image capture, the SXGA read noise is < 20 e⁻ to 25 MHz. In the higher gain mode, the SXGA's read noise is < 10 e⁻ to 20 MHz.

Also plotted in the figure are the theoretical limits for CCD noise at C_{sense} of 8 fF. The CCD noise data culled from catalogues are roughly a factor of 2 higher from this practical limit. In generating these theoretical limits we assumed that 10 time constants of settling time are needed to properly sample the data for subsequent digitisation [6]. Since further improvements in CMOS imager read noise can be readily achieved as the technology matures as evidenced by the buffered gate modulation results at < 1 e⁻ independent of frequency, the fundamental superiority of CMOS imagers has been validated. CMOS imagers should therefore initially supplant CCDs for large formats and eventually migrate to smaller formats as the technology evolves and deep submicron lithography becomes available.

6. Conclusions

The theoretical advantages of CMOS-based imagers have been validated on infrared and visible FPAs. While the read noise of competing CCD imagers has not improved significantly over the last decade except when the video rate is slowed to rates unacceptable for most applications, CMOS devices are rapidly improving and have already yielded superior performance, including lower read noise and higher sensitivity. CMOS visible imagers already provide read noise below 10 e⁻, while the more advanced infrared imagers provide

< 1 e^- read noise. Coupled with their superior sensitivity, it appears that CMOS imagers are likely to supplant CCDs for many applications.

References

1. L.J. Kozłowski, "Attributes and drawbacks of submicron CMOS for IR FPA readouts", *Proc. SPIE* **3360**, April (1998).
2. A. Rogalski, "Recent progress in HgCdTe infrared detector technology", *Opto-Electronics Review* **6**, 47–67 (1998).
3. K.W Hodapp, J.L. Hora, D.N.B. Hall, L.L. Cowie, M. Metzger, E. Irwin, K. Vural, L.J. Kozlowski, S.A. Cabelli, C.Y. Chen, D.E. Cooper, G.L. Bostrup, R.B. Bailey, and W.E. Kleinhans, "The HAWAII infrared detector arrays: testing and astronomical characterisation of prototype and science-grade devices" *New Astronomy* **1**, 177–196 (1998).
4. L.J. Kozłowski, "3.2 μm PACE-I HgCdTe 1024×1024 FPA", *188th Electrochemical Society Meeting*, October (1995).
5. K. Vural, L.J. Kozlowski, D.E. Cooper, C.A. Chern, G. Bostrup, C. Cabelli, J.M. Arias, J. Bajaj, K. Hodapp, D.B. Hall, and W.E. Kleinhans, "2048×2048 HgCdTe focal plane arrays for astronomy applications", *Proc. SPIE* **3698**, 24–35 (1999).
6. L.J. Kozłowski and J. Luo, "Comparison of passive and active pixel sensors for CMOS visible imagers", *Proc. SPIE* **3360**, April (1998).
7. J.F. Johnson, "Hybrid infrared focal plane signal and noise model", *IEEE Trans. Electron Devices* **46**, 96–108 (1999).
8. L.J. Kozłowski, S.A. Cabelli, D.E. Cooper, and K. Vural, "Low background infrared hybrid focal plane array characterization", *Proc. SPIE* **1946**, 199–213 (1993).