Contributed paper

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Design and implementation of infrared readout circuit using a new input circuit of current mirroring direct injection (CMDI)

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A new readout structure for infrared (IR) focal plane arrays (FPA) is presented in this paper. By applying a new input circuit of current mirroring direct injection (CMDI), we realised a high-performance readout circuit for IRFPA. It was found from the SPICE simulation that the CMDI inherently makes the detector bias stable as well as has almost 100% injection efficiency to the readout circuit from the detector even for low R_DA values because it has almost zero input impedance. Compared with previous other input circuits, it has also many advantages such as small area and low power consumption. A readout chip including the CMDI input circuit has been designed and fabricated for MWIR 1×128 staggered linear HgCdTe infrared detector arrays using 1.2 μm single-poly-double-metal N-well CMOS technology. From the measurement results of the fabricated chip, the readout function was successfully verified at 77 K with 5 V supply voltage.

Keywords: readout integrated circuit (ROIC), infrared detector, new input circuit, current mirror.

1. Introduction

Key to the development of today's readout integrated circuits (ROIC's) has been the evolution in input circuit (preamplifier) design. This evolution has been driven by increased performance requirements and silicon processing technology improvement [1].

Direct injection (DI) circuit, shown in Fig. 1(a), is one of the first integrated readout preamplifiers for second generation detectors and has been used as an input to CCDs for many years [1]. The detector current (I_{ph}) charges the integration capacitor (C_{INT}) which in turn determines the gain. It can be fabricated in small area (< 20 μm × 20 μm). The detector bias remains relatively constant at medium to high irradiance backgrounds, providing sufficient photo-current to maintain high MOSFET transconductance (g_m), which results in low detector input impedance and stable detector bias. At small photocurrent, however, the MOSFET's transconductance decreases substantially and thereby the injection efficiency drastically decreases.

Direct injection circuit perform photocurrent integration through the channel of an active transistor or CCD channel. Usually the detector node voltage is not reset directly; rather, charges accumulated on the integration capacitor (or CCD bucket) on the output of the injection transistor, are reset or transferred periodically. The DI has a linear response over the applicable range and is widely used in visible CCD imagers. To reduce detector noise, near-zero bias should be maintained across all detectors, however this is not possible due to the threshold variation in the input channels.

A buffered direct injection (BDI) circuit, shown in Fig. 1(b), uses an inverting amplifier to reduce the input impedance, thus improving injection efficiency, bias stability, and frequency response. It can maintain relatively constant detector bias at medium and high backgrounds. The minimum operating photon flux range of the BDI is approximately an order of magnitude smaller than that of the DI. However, the BDI requires larger unit cell real estate than the DI circuit with increased power dissipation. And the detector bias variation due to the threshold voltage variation

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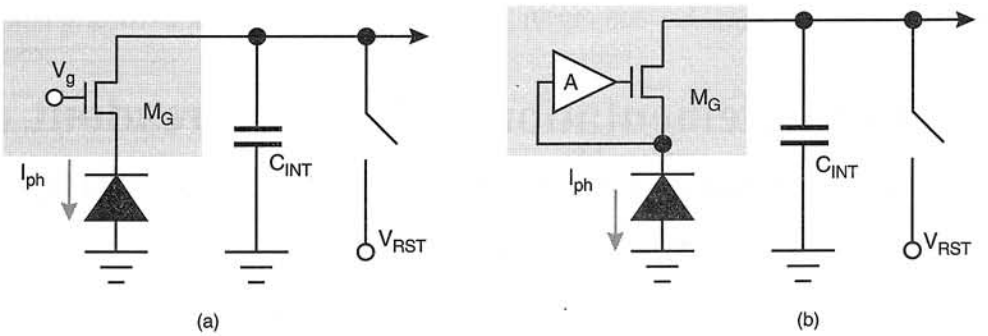

Fig. 1. Direct injection (DI) (a) and buffered direct injection (BDI) circuit (b), where I_{ph} is the detector photo-current induced by IR illumination, C_{INT} is the integration capacitor, and V_{RST} is integrator reset voltage.

decreases with higher inverting amplifier gain, but it is still difficult to maintain zero bias across all the detectors because the amplifier offset voltage varies from cell to cell. The detector bias variation will bring non-uniformity and increased noise.

To maintain zero bias across the detector, we previously proposed a new input circuit, named current mirroring direct injection (CMDI) in Ref. 2 as shown in Fig. 2. We could show that this new input circuit has also many other advantages, such as high injection efficiency, low power consumption, and small unit cell area, over the BDI approach [2]. Using this newly proposed input circuit, we have realised the entire readout integrated circuit for MWIR 1×128 staggered linear HgCdTe photodiode arrays.

2. Readout integrated circuit (ROIC) implementation

When a couple of MOSFETs in a current mirror are completely matched, the same drain currents (ID) will flow through the two MOSFETs. Subsequently, when the same drain currents flow through a couple of MOSFETs with the same geometry, their V_{GS} should be equal. With this concept, we use two NMOSFETs, M_{n1} and M_{n2} with the same size, as shown in Fig. 2(a). If the currents through them are equal, the source voltage of M_{n2} should be zero because the gate nodes of them are tied. Thus the detector bias is maintained at zero voltage. To make the same currents flow through M_{n1} and M_{n2}, a PMOSFET current mirror with M_{p1} and M_{p2} is connected to the NMOSFET current mirror. The photocurrent, I_{ph} induced by infrared (IR) illumination flows through M_{n2} and M_{p2}. Then, by current mirroring of M_{p1} and M_{p2}, the same current will flow through M_{p1} and M_{n1}, thereby the drain currents of M_{n1} and M_{n2} are equal to each other. As mentioned above, the detector bias will be fixed to zero.

In the circuit of Fig. 2(a), the amount of the current integrated in the capacitor C_{INT} is the sum of I_{ph} and the current flowing through M_{n1} (and M_{p1}). However, there will be problems arising from possible threshold voltage mismatches. Even small threshold voltage mismatch between M_{p1} and M_{p2} induces a large difference in their drain currents when they operate in the subthreshold region. Therefore, there may be non-uniformity in the integrated current even under uniform illumination. So, we proposed an improved version as shown in Fig. 2(b), where the integration capacitor is placed between the M_{n2} and M_{p2}, hence only the photo-current, I_{ph}, will be

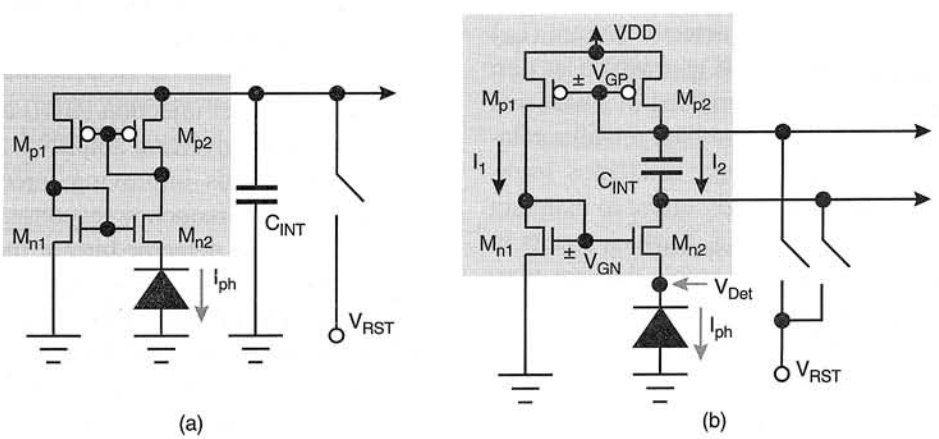

Fig. 2. New unit cell of current mirroring direct injection circuit (CMDI) (a) and the improved version of (a) (b).

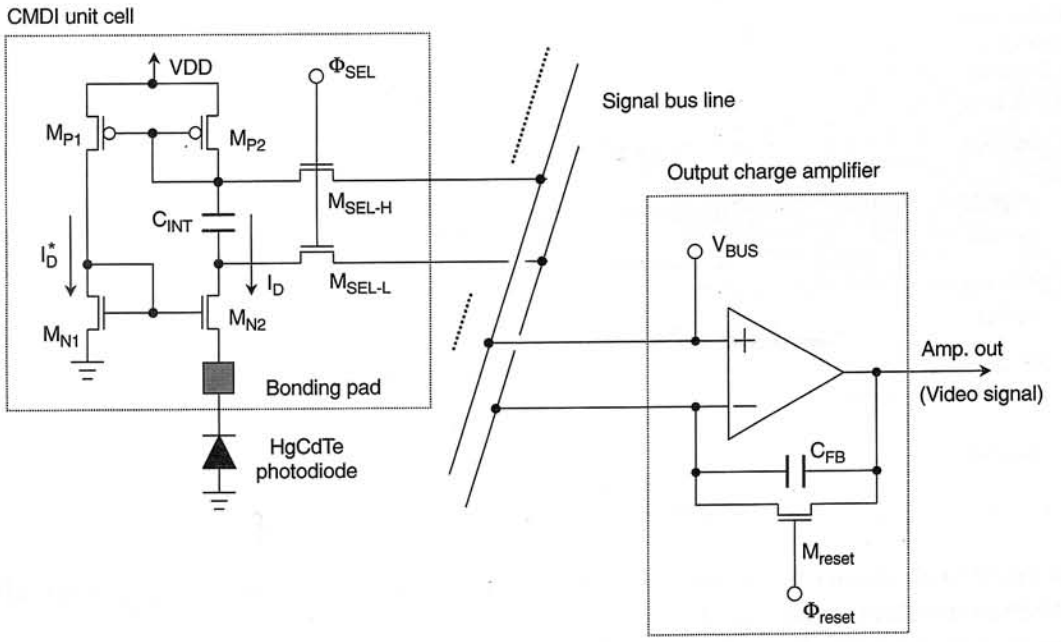

Fig. 3. Schematic diagram of 1×128 linear current mirroring direct injection (CMDI) readout circuit.

integrated. In this case, the V_T mismatch does not affect the uniformity. Using this improved version of CMDI input circuit, we designed the entire readout integrated circuit for MWIR 1×128 staggered linear HgCdTe photodiode arrays. CMDI input circuit needs 4 transistors and 2 more transistors as pixel selection switches. It is a smaller number of transistors than BDI circuit needs when BDI input circuit adopts a differential amplifier as an inverting amplifier to get a high gain (7 transistors). A schematic diagram of the new readout circuit is shown in Fig. 3. In this circuit, the electrical value processed by the readout circuit is neither the current, nor the voltage, but charge obtained by pre-integration of the current delivered from the detector into the pixel integration capacitor (C_{INT}) of input circuit then by reading this charge using an output charge amplifier. The charge amplifier is connected to the end of signal bus lines.

Since the signal bus lines are designed to be kept at a constant potential (V_{BUS}) by the charge amplifier whose input impedance is assumed to be infinite, the current impulse caused by the injection of charges is converted into a voltage output by the output charge amplifier and a feedback capacitor (C_{FB}). Its output can then be directly the video output to be processed.

The n-th pixel voltage output V(n) at the output of the charge amplifier is given by the expression

$$V(n) = I_D(n) \times T_{INT}/C_{FB}\,, \qquad (1)$$

where C_{FB} is the feedback capacitance of the charge amplifier, $I_D(n)$ the photocurrent of n-th detector, and T_{INT} the integration time.

One should note that the capacitance of the bus lines do not intervene in the transfer of charge from C_{INT} to C_{FB} since the charge amplifier is a differential input type with very large gain over 1000. Because the bus lines are being kept at a constant potential by this amplifier, its voltage is constant however large the parasitic capacitance of the bus lines is. In Eq. (1), it should be also noted that C_{INT} is not contained. Therefore the cell to cell non-uniformity of C_{INT} dose not affect the signal output. It is also one of the big merits of this circuit architecture.

The addressing transistors M_{SEL-H} and M_{SEL-L}, when in 'OFF' state, isolate C_{INT} from the bus so that no charge is exchanged between the bus and the integration capacitor of the pixel. After the switches are turned off, C_{INT} is isolated from the bus lines and photocurrent integration begins.

The signal bus lines are connected to a differential amplifier with C_{FB} feedback capacitor. The non-inverting input of the charge amplifier is connected to a V_{BUS} power supply. The gate signal of the addressing transistors M_{SEL-H} and M_{SEL-L} is provided by on-chip CMOS shift register. When these transistors are turned on, both of the node voltages, i.e., high and low node of C_{INT}, will be same as V_{BUS}, and the pre-integrated charge which existed in C_{INT} is transferred to C_{FB}, the feedback capacitor of the charge amplifier. The reset switch, which is connected parallel to C_{FB}, resets the feedback capacitor to be ready to read the integrated photon charge of the next cell.

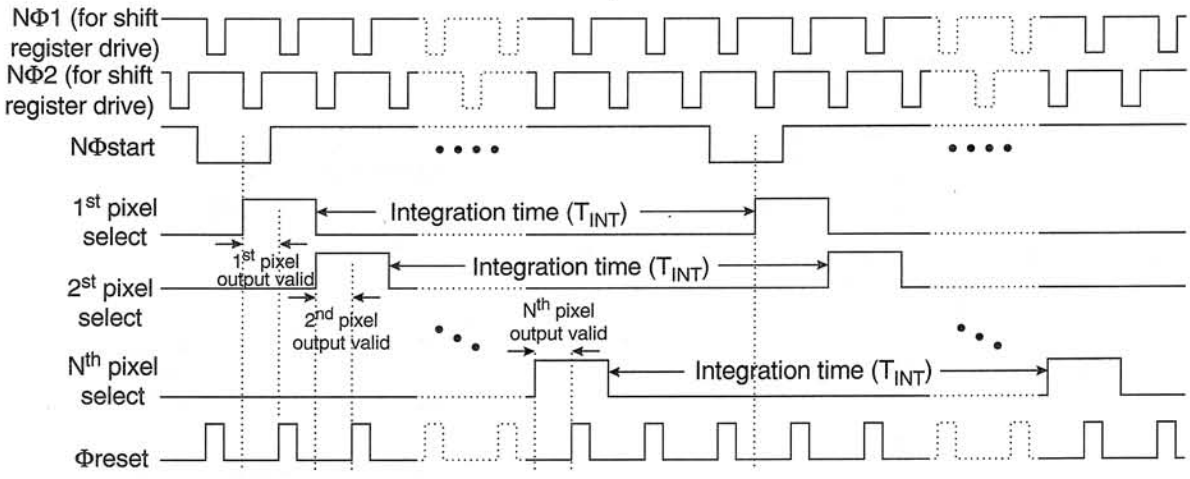

Fig. 4. The clock timing waveform of circuit driving clocks.

More detailed clock timing waveforms are shown in Fig. 4. Each of the clock signals has a high level of 5 V and low a level of 0 V. In this figure, the first and second clock signals are pair of non-overlapping 2-phase negative input clocks to be used for driving the on-chip CMOS shift register. The pixel period will be determined by the period of NΦ1 (or NΦ2). The third waveform, NΦstart, represents the negative input clock signal of the shift register. After the low level of NΦstart signal with one period of NΦ1 (or NΦ2), the pixel selection signals become high sequentially by the CMOS shift register as shown in the 4, 5 and 6th waveforms of the figure. These pixel selection signals will be connected to the gates of addressing transistors $M_{SEL\text{-}H}$ and $M_{SEL\text{-}L}$ in Fig. 3. During a pixel period the integrated charge should be transferred to the C_{FB} and then C_{FB} should be reset for the readout of next cell. The last waveform of Fig. 4 shows the C_{FB} reset signal, Φreset. We used the inverting signal of NΦ1 as this reset signal for the design simplicity.

The differential amplifier must satisfy the following requirement [3]:

- the output voltage range should be as large as possible in order to maximise its charge to voltage conversion factor,
- the open loop gain should be large enough to maintain the column bus at a constant potential during the readout of charge stored in a pixel,
- the power consumption needs to be very low in order to minimise the cooling requirement,
- the frequency bandwidth needs to be wide enough to achieve high pixel data rate.

To satisfy these requirements, we choose a folded cascade type CMOS differential amplifier as the output charge amplifier. The circuit diagram is shown in Fig. 5.

3. ROIC simulation and experimental results

Figure 6 shows the SPICE simulation results of the node voltages of the integration capacitor, C_{INT} during the integration time of T_{INT} = 69 μs in the readout circuit with the input current signals of 10 nA, 20 nA, 30 nA, 40 nA, and 50 nA and the integration capacitance of 2 pF. The simulations were performed using the device parameters of 1.2-μm single-poly-double-metal n-well CMOS technology at 77 K. As shown in Fig. 6(a), Vc_H, the upper node voltage of integration capacitor does not move during the integration while Vc_L, the bottom node voltage of the integration capacitor is discharged with different discharging rates proportional to the input current. Figure 6(b) shows pixel selection signal (Φsel), feedback capacitor reset signal (Φreset), integration capacitor voltage [same as Fig. 6(a)] and amplifier output voltage with

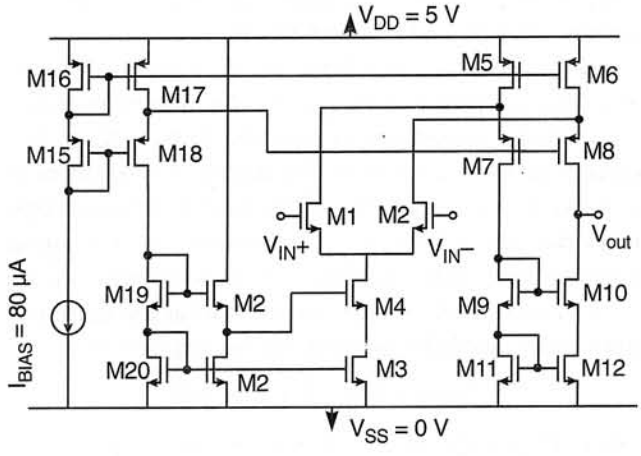

Fig. 5. Folded cascode CMOS differential amplifier as the output charge amplifier.

magnified time scale concentrated on the pixel selection timing. When the pixel selection signal goes to high, both of the integration capacitor node voltages, Vc_H and Vc_L, become the same voltage of V_{BUS} (= 2.5 V). At the same time, the integrated charge of C_{INT} is transferred to C_{FB}. The amount of transferred charge is appeared as the output voltage of amplifier as shown in the fourth waveform of Fig. 6(b).

An experimental 1×128 CMDI readout chip has been designed and fabricated to verify the proposed new input circuit structure. The photograph of the readout chip fabricated with 1.2-μm single-poly--doule-metal (SPDM) n-well CMOS technology is shown in Fig. 7. The total chip size is 4×7 mm^2. This chip is designed for MWIR 1×128 staggered linear HgCdTe photodiode arrays to operate with 5 V-power supply for both analogue and digital circuit operations. In readout circuit, 1×128 staggered linear array

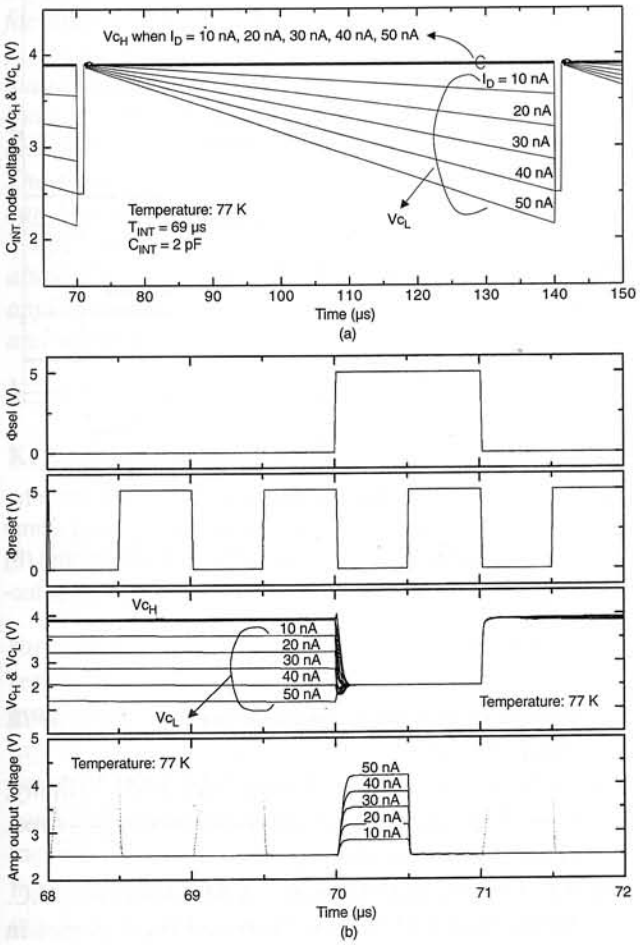

Fig. 6. Simulated waveforms of the designed 1×128 CMDI readout chip: (a) discharging waveforms of the integration capacitor C_{INT} during the integration time with various detector photo-currents from 10 nA to 50 nA with 10 nA step, (b) switching and output waveforms with magnified time scale concentrated on the pixel selection timing.

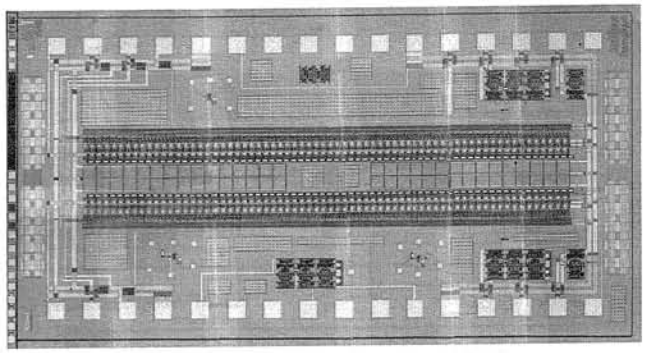

Fig. 7. Photograph of fabricated 1×128 CMDI readout chip.

configuration is realised by 2×64 (actually 2×68 with four extra dummy pixels) configuration and has two (left/right) output channels including two output amplifiers. The signal timing between two channels is designed for proper readout of staggered pixels. The detector pixel size is 40×30 μm^2 and the pixel pitch and staggered pitch are 80 μm and 90 μm respectively. And the fabricated chip has a maximum charge storage capacity of 2.5×10^7 electrons. The chip was packaged and tested in a vacuum Dewar at 77 K. It was also tested under room temperature. The experimental results are shown in Fig. 8 to Fig. 9. Figure 8 shows the shift register driving clocks, pixel selection signals and amplifier output waveforms of the both output channels during an integration period. The clock (NΦ1 and NΦ2) frequency is 10 kHz and the integration time is 8 ms. The measured discharging waveforms of the integration capacitor, C_{INT} are shown in Fig. 9. We can see these measurement results show the same waveforms as those of the simulation results.

4. Conclusions

In this paper, a new CMDI readout structure for IRFPA was proposed, analysed and experimentally verified. In the new readout circuit, the Current Mirroring Direct Injection (CMDI) input circuit was adopted. The CMDI input circuit can control detector bias automatically and almost 100% injection efficiency can be obtained even for low R_DA values because we can achieve nearly zero input impedance in this new input circuit. Compared with previous other input circuits, it is expected to have also many advantages such as small area, low power consumption and detector bias stability. The function and performance of the proposed CMDI readout structure has been verified by SPICE simulation and the measurements on a readout circuit designed and fabricated for MWIR

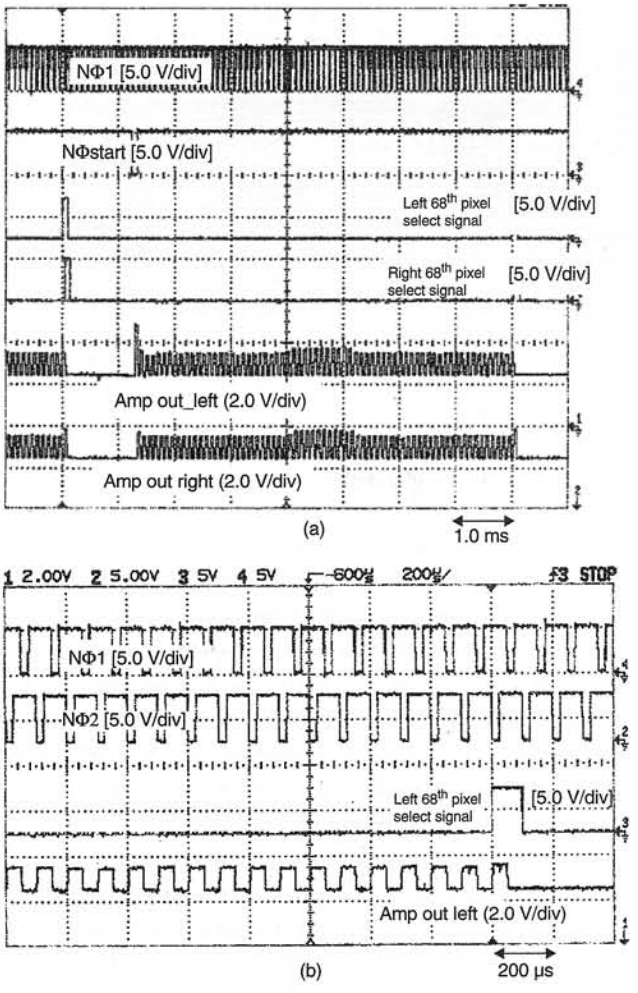

Fig. 8. The measured waveforms of the fabricated 1×128 CMDI readout chip: (a) during the one-line period (same as integration period) with driving and switch signals and (b) with magnified time scale concentrated on the pixel selection timing.

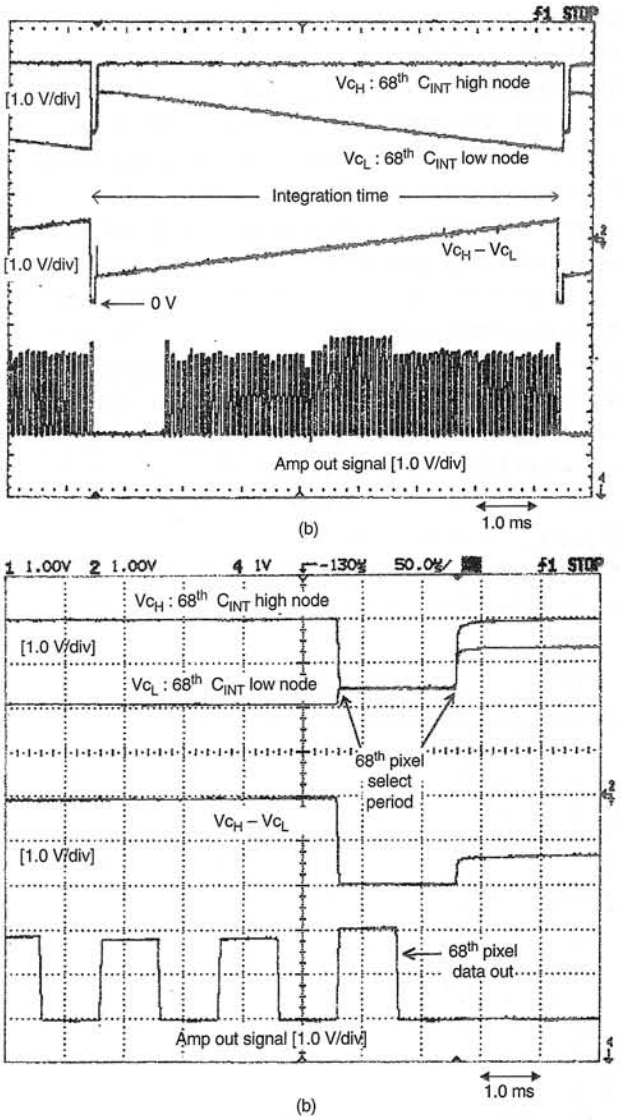

Fig. 9. The measured discharging waveforms of the integration capacitor C_{INT}, (a) during the one-line period (same as integration period) with driving and switch signals and (b) with magnified time scale concentrated on the pixel selection timing.

1×128 staggered linear HgCdTe infrared detector arrays using 1.2-μm single-poly-double-metal N-well CMOS technology.

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