OPTO-ELECTRONICS REVIEW **8**(4), 299–306 (2000)

Advanced concepts of industrial technologies of crystalline silicon solar cells

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This paper reports on the results of several years of investigations aiming at simplification and efficiency improvement of a low cost screen printing solar cell process. All solar cell process operations, materials and equipment have been, with this respect, critically examined, re-optimised and, if necessary, removed or replaced. A simple industrial type process for high efficiency multicrystalline and monocrystalline solar cells has been developed. The process sequence is based on screen printed contacts fired through a PECVD SiNx antireflection coating layer. The total number of processing steps has been reduced to six. All processing steps can be easily transferred into big volume production lines. Solar cells with average cell efficiency above 15% and 17% were respectively obtained on large area multicrystalline and monocrystalline substrates. Including in the processing sequence the advanced processes of isotropic texturisation and selective emitter increases the cell efficiency to 16.9% and 17.9% respectively for multi- and monocrystalline silicon. A new cell concept, metallisation wrap through cell (MWT), has been recently introduced. The cell efficiency of 13.1% has been obtained in a simple cell processing sequence based on screen printed contacts.

Keywords: solar cells, crystalline silicon, manufacturing and processing.

1. Introduction

Typical efficiency of commercially produced crystalline silicon solar cells lies in the range of 13–16%. Generally, accepted future efficiency goals for industrial solar cells are 18–20% on monocrystalline and 16–18% on multicrystalline silicon. Although it is well known how to manufacture the high efficiency laboratory cells, direct transfer of these processes to production lines is impossible due to several processing bottlenecks. The laboratory processes aim usually at obtaining the maximum efficiency with a cost issue being of secondary importance. Contrary to that, industrial processing techniques and materials are selected for the maximal cost reduction while maintaining a relatively good efficiency. The high value of the performance/cost ratio is the main concern of industrially manufactured PV systems. Industrial solar cells are fabricated in large volumes mainly on large area (100–225 cm^2) Czochralski monocrystalline or multicrystalline silicon substrates. The production processes and equipment should fulfil throughput requirements of more than 1000 wafers per hour. Most of the high efficiency processing steps developed on a laboratory level did not take into account the high throughput requirement. There is therefore a big gap between cell efficiencies reported by research laboratories and PV industry.

For the last few years IMEC is being engaged in several projects, founded mostly by the EC Joule Programme, aiming at improvement of an industrial solar cell process based on screen printed metallisation. Since most of the current crystalline silicon solar cell production lines are based on this technology, developed processing steps can be directly implemented into industry without excessive investments.

This paper summarises the research and development efforts undertaken in IMEC during the last few years towards development of a high efficiency low cost industrial solar cell process. The basic working principle is that all developed processes should be industrially compatible. In the first phase, all solar cell process operations and materials had been, with this respect, critically examined, re-optimised and, if necessary, removed. In the next phase, we concentrated on the development of new materials, processes and equipment which should lead to an improved cell efficiency but cell fabrication should be kept simple, robust, easy to be automated, economic and as much as possible operator independent. This resulted in a simplified industrial solar cell process based on a screen printed metallisation fired through a PECVD silicon nitride layer. This process is now directly transferable into industrial mass production lines. Several new advanced processes, not mature yet for implementation in industry, are being still under intensive testing in the pilot line.

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2. Processing step optimisation

2.1. Texturisation

Surface texturing reduces the optical reflection from the single crystalline silicon surface to less than 10% by allowing the reflected ray to be re-coupled into the cell. Monocrystalline silicon substrates with a surface orientation <100> can be textured by anisotropic etching in a weak solution of NaOH or KOH with addition of isopropanol resulting in randomly distributed pyramids. Important is to control the pyramid size since it has influence on the cell processing and finished cell performance. Uniformly distributed pyramids with height of 3–5 µm are optimal for low reflection losses and help in obtaining a good quality screen printing metallization process [1].

The random texturisation process is not effective on multicrystalline substrates due to its anisotropic nature. The different grain orientations inhibit a uniform texturisation thereby limiting the short circuit current of multicrystalline solar cells. Different techniques like mechanical V-grooving, isotropic wet-acid etching, electro-discharge machining (EDM) and reactive ion etching are being currently investigated. The mechanical V-grooving, i.e., forming V-grooves in Si wafers by mechanical abrasion, using a conventional dicing saw and beveled blades, has evolved from a single blade laboratory technique to a multi-blade, high throughput process being ready for industrial implementation [2]. The structure of a mechanically V-grooved silicon surface is shown in Fig. 1.

Although V-grooved multicrystalline silicon surface has the lowest reflectance and consequently the highest short circuit currents can be obtained, there is still, a manufacturability problem related to an incompatibility of screen printed metallisation process on deeply grooved surfaces. This problem can be solved by applying alternative metallisation techniques like electroless plating or roller printing [3]. The still remaining problem is the high wafer breakage occurring in the cell process when V-grooving is applied to texture wafers with the thickness below 200 µm.

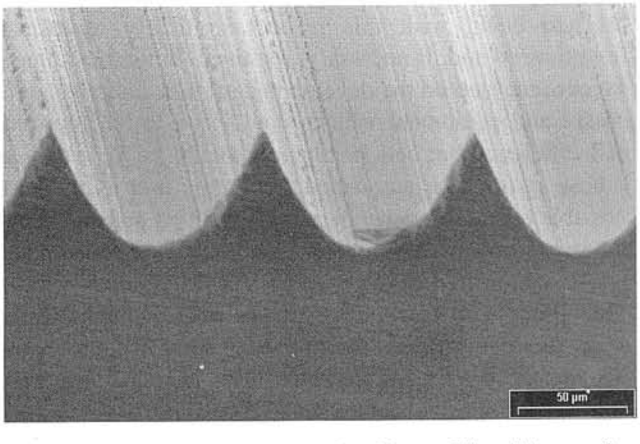


Fig. 1. SEM picture of V-grooved multicrystalline silicon wafer.

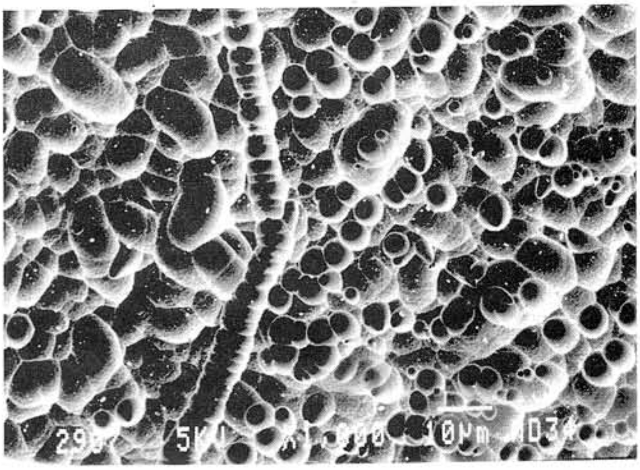


Fig. 2. SEM picture of isotropically acid etched multicrystalline silicon surface.

Contacting and breakage problems can be avoided by applying alternative processes like isotropic acid etching [4], reactive ion etching (RIE) [5]. The proprietary acid solution combines the removal of saw damage and the texturing itself in one single relatively short process step [4]. The resulting microstructures in combination with an antireflection coating decrease the surface reflection to a value significantly below randomly textured multicrystalline-Si wafers. Figure 2 presents the SEM picture of an isotropically etched multi-Si wafer. Consequently, a 4% increase in J_{sc} has been measured on finished multicrystalline solar cells. Due to the macroscopically flat surfaces after texturing, and increased metallisation contact area on the top of microscopically textured surfaces, fill factors above 77% are regularly achieved with screen printed metallisation. Summarising all contributions a 0.4% absolute increase in efficiency is regularly achieved with reference to randomly alkaline textured wafers. Unfortunately this etching process produces a relatively large amount of chemical waste giving rise to additional processing costs, which have to be balanced against the gains in efficiency and the simplification of the process sequence. In terms of mechanical yield, reproducibility and batch size, acidic texturing is fully comparable with alkaline texturing.

Plasma etching, unlike mechanical grooving and acid etching, is contact free and dry etching technique. In a reactive ion etching process silicon wafers are exposed to a direct chlorine plasma. By controlling the gas flow, RF power and reaction pressure homogenous pyramid-like structures are formed on the surface of multicrystalline silicon wafers (see Fig. 3) [6]. The implementation of RIE for a front surface structuring of multicrystalline wafers is at the age of an industrial implementation and high throughput production systems are under construction. High efficiency solar cells close to 17% have been already reported [5].

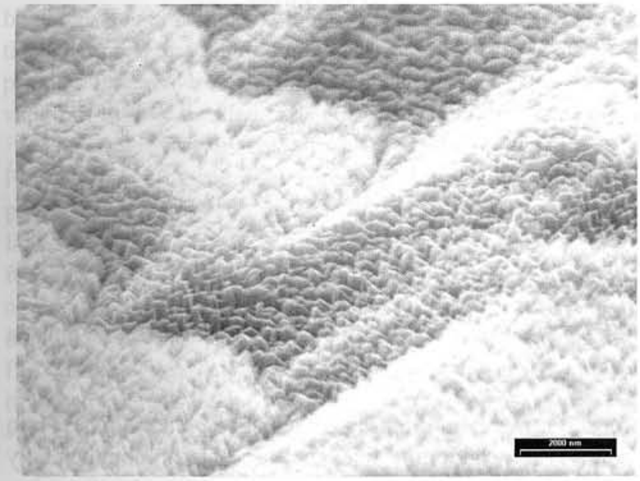


Fig. 3. SEM picture of isotropically RIE etched multicrystalline silicon surface.

2.2. Cleaning

Silicon wafer cleaning is not often discussed in the solar cell technical literature. Long diffusion lengths of minority carriers, necessary for high efficiency cells, require low levels of metal contamination on the silicon surface before a high temperature treatment. The lengthy and costly RCA pre-oxidation and pre-diffusion cleaning sequence is still often used in high efficiency laboratory solar cell processing. There is however, a growing concern among the PV community related to large amounts of chemical waste products resulting from solar cell processing. The approach towards wafer cleaning followed in this work, the so-called "just-clean-enough" concept has been borrowed from the ultra-clean processing research of IMEC. Very often, the same performance of solar cells can be achieved by a much more cost effective cleaning sequence. The basic principle is to precisely define what type of contaminants have to be removed and then look for the most cost effective cleaning process. In the case of the laboratory solar cells where many photolithographic processes and prolonged high temperature steps are implemented, one needs to get rid of particles of any type, organic and metallic contaminants. In this case, the traditional RCA cleaning sequence can be replaced by the "IMEC-clean" [7], which usually consists only of an H_2SO_4/H_2O_2 step, followed by a diluted HF step. "IMEC-clean" used to be applied before the high temperature steps in a cell process like diffusion and dry oxide passivation. More detailed evaluation showed that the excessive cleaning does not result in a better efficiency of industrial solar cells therefore the "RCA-cleaning" and "IMEC -clean" sequences could be removed from cell processing.

The industrial solar cell process of crystalline silicon solar cells is free of photolithographic processes and long processing steps at high temperatures. The first wafer cleaning is performed after an alkaline texturing and before a diffusion step. In this case, neutralisation of sodium or potassium traces and removal of metallic contamination is the only issue. A cleaning sequence consisting of only 1–5% diluted HCl at 90°C and followed by diluted HF step yields excellent results. If the diffusion process is carried out in an open quartz tube furnace using $POCl_3$ as a phosphorus source, a short dip in diluted HF is the only step needed before a dry oxidation process. In case of the IMEC cell process, PECVD silicon nitride plays role of an ARC and passivating layer. This allows avoiding a dry oxide passivation step and related to it wet cleaning. Moreover, diffusion glass is kept on the wafer surface. The final cell process contains only three wet chemical processing steps: saw damage etching, texturisation and neutralisation in hot diluted HCl. This so-called "HF-free cleaning" has been introduced in a solar cell process giving the same cell efficiencies as more costly and complex cleaning sequences resulting in a considerable reduction of chemical waste products leading to important cost savings and environmentally friendly cell processing. The evolution of solar cell processes, related wet-cleaning steps and cost savings are presented in Table 1.

Table 1. Evolution of solar cell processes and related wet-cleaning steps.

Wet-chemical process	Chemicals used – number of chemical baths	Savings (BEF/waf)
1. Reference process: texturisation, Na neutralisation in HCl, HF dip, pre-diffusion IMEC-clean, diffusion glass etching, pre-oxidation IMEC clean	NaOH – 2, HCl – 1, HF – 4, H_2SO_4/H_2O_2 – 2, DI water – 9 Total: 18 baths	–
2. Like in 1 above but without pre-difussion cleaning	NaOH – 2, HCl – 1, HF – 3, H_2SO_4/H_2O_2 – 1, DI water – 7, Total: 14 baths	2.62
3. Like in 2 above but without pre-oxidation cleaning	NaOH – 2, HCl – 1, HF – 2, DI water – 5 Total: 10 baths	5.24
4. Like in 3 above but without HF dip and diffusion glass etching.	NaOH – 2, HCl – 1, DI water – 3 Total : 6 baths	5.71

2.3. Industrially applicable processes for high quality emitters

The common industrial cell process based on screen printed metallisation has usually a deeply diffused and non-passivated emitter with a high phosphorus surface concentration, giving rise to a poor response to short wavelength light. Consequently, the top region of the emitter acts as a dead layer for the generated minority carriers. In this work two approaches have been tried to improve the cell "blue response": shallow, uniform and well-passivated emitter and secondly selective emitter combined with screen printed metallisation. The optimisation of the homogeneous emitter diffusion is directly linked to the metallisation process described below. Very good results have been achieved by modifying the composition of the front contact paste and by applying fast firing of screen printed contacts in IR or RTP furnaces. There are successful reports of high fill factors obtained by a screen printing process on high sheet resistance emitters. Efficiencies above 15% were obtained by contacting a 100 Ω/sq. emitter by firing-through-SiN_x onto an RIE-textured surface [8].

Another direction, which is followed in IMEC, is development of an industrially applicable selective emitter process. A shallow emitter between the metal grid combined with an effective surface passivation reduces the emitter dark saturation current, and a deep emitter beneath unpassivated regions such as the metal-Si interface gives rise to low resistive contacts. Different selective emitter concepts have been established at laboratory level. Most of them require relatively complicated or expensive processing steps and are not attractive for industrial production. One exception is the conventional laser-grooved buried contact process, which utilises selective emitters in industrial solar cell manufacturing [9].

A very promising approach towards an industrial selective emitter concept, which can be implemented in screen printing production lines, is based on a single-step selective diffusion from screen printed P-doping paste. This technology [10] basically involves screen printing of a doping (phosphorous) paste onto the wafer in the form of a finger pattern (i.e. by using a screen similar to that for metallisation) with some tolerance for alignment, and performing the diffusion in a belt furnace. The areas where the doping is directly deposited are deeply diffused whereas the areas in between the "fingers" are shallowly diffused due to the gas phase transportation of the doping in the belt furnace. Figure 4 shows a scheme of this diffusion principle. The advantage is that the process does not require any additional masking or etching steps. An excellent surface passivation is obtained by applying a PECVD SiN_x ARC layer in combination with a firing-through process as described later. This technology is especially suited for screen printed solar cells but requires an alignment during the screen printing of the front metal contact. Industrially compatible, high-throughput screen printing systems equipped with digital cameras are now commercially available with precise alignment facilities. One still remaining problem for the implementation of this selective emitter process into solar cell production lines is the lack of commercially available stable screens. However, the latest developments in stencil screens give strong indications that durable screens without deformation during production will soon be commercially available [11].

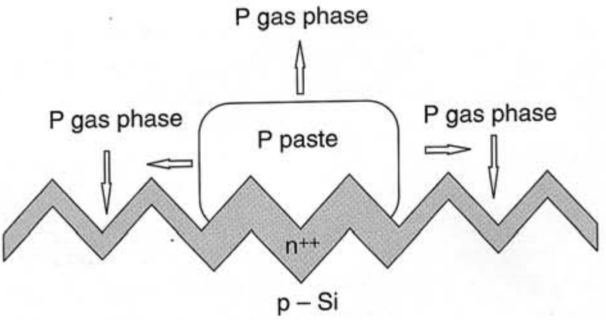


Fig. 4. Scheme of selective emitter process from screen printing P-paste.

2.4. ARC and metallisation

ARC layers of TiO_x and SiN_x have been examined for their suitability and performance after encapsulation. It has been found that the refractive index of TiO_x can be increased from 1.9, directly after an APCVD process, to a more optimal value for encapsulation of 2.3 if a thermal treatment at temperatures above 700°C is applied. In case of PECVD SiN_x ARC the refractive index can be controlled by the flow ratio of silane and ammonia in the deposition process. It has been proven that a thermal treatment of silicon nitride after the deposition gives a perfect surface and bulk passivation thanks to the release of hydrogen at temperatures of 600–800°C [12].

Figure 5 displays the absorption spectrum for the deposited and the annealed nitride layer. The bonding concentrations can be calculated from these spectra. A relative decrease of 10% and 37% for respectively the Si-H and N-H

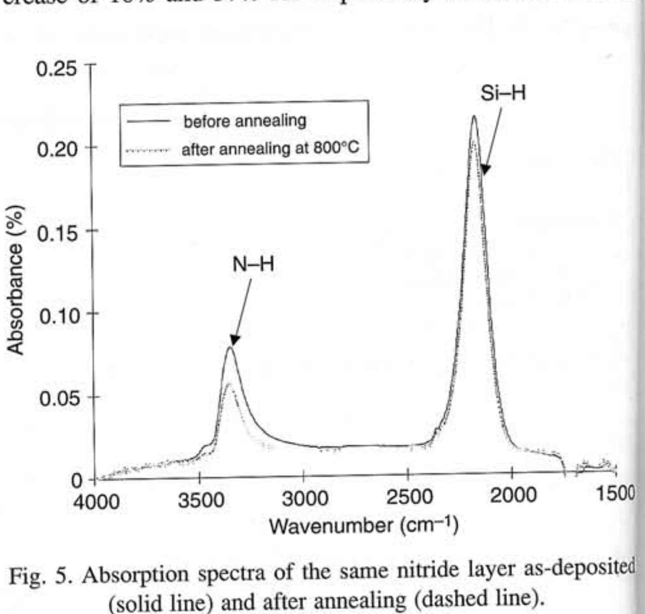


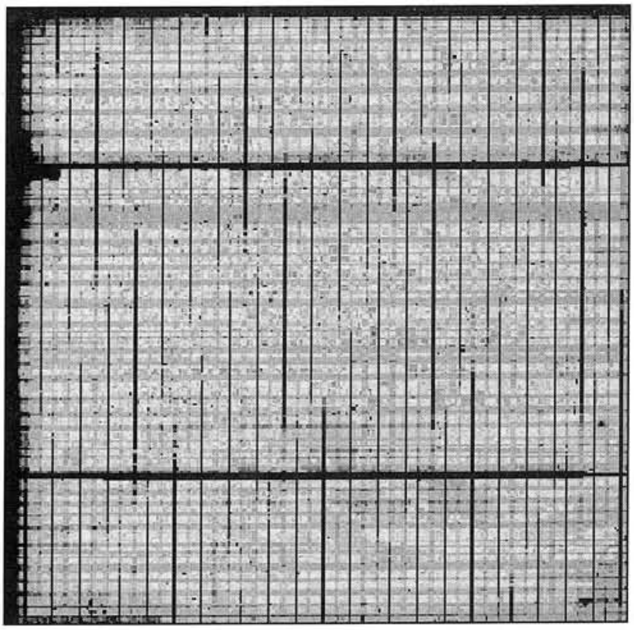
Fig. 5. Absorption spectra of the same nitride layer as-deposited (solid line) and after annealing (dashed line).

bondings by annealing the layer [13] has been observed. If this phenomenon could be integrated in a simple screen printing process, a cost-effective technique for the passivation of multicrystalline cells could become available.

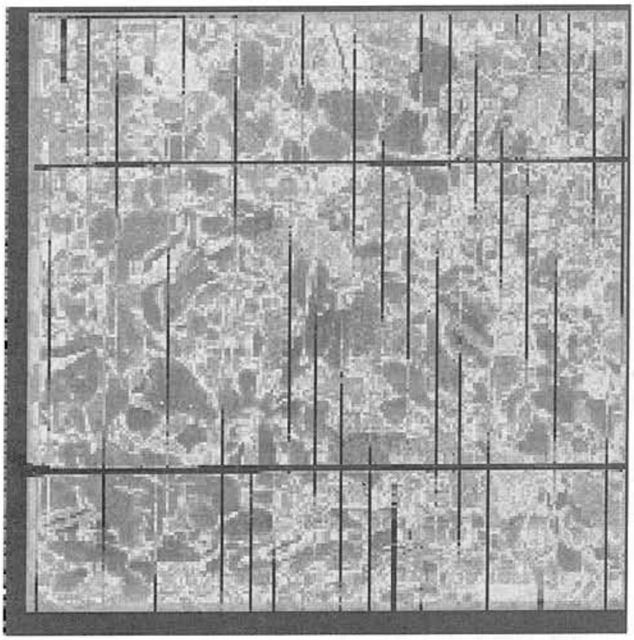
The beneficial effect of the thermal treatment of PECVD can be combined with the firing step of screen printed front contacts if one can fire-through silicon nitride layer. Many samples of silver pastes specially formulated for this purpose have been tested. Precise selection of paste compositions and well-trimmed firing process resulted in a metallisation process with simultaneous firing-through a PECVD SiN_x layer. This process has a number of additional advantages [14]:

- front contacts are not covered by ARC and can be directly soldered,
- hydrogen released from SiN_x layer at elevated temperature gives excellent surface and bulk passivation, thanks to that the dry oxidation step can be omitted,
- the high firing temperature makes possible the simultaneous formation of an Al-alloyed BSF,
- the PECVD SiN_x layer slows down the aggressive etching of silicon by molten glass frit.

As a result one processing step of contact firing-through PECVD SiN_x combines the functions of a few separate processing steps: front and back contact firing, surface and bulk passivation, Al-BSF formation and additionally screen printed contacts with high fill factors can be fabricated on shallow and well passivated emitters. The bulk passivation properties of this process are particularly attractive since there are no other industrial alternatives. Thanks to all these benefits, high efficiency solar cells can be fabricated by a low cost screen printing process. The passivating properties of this process have been studied by laser beam induced current (LBIC) measurements [15] (see Fig. 6). Typical multicrystalline cells made with the firing through silicon nitride process have shown the uniform passivation of the surface and the upper part of the bulk, independently of the grain orientation. For short wavelengths [Fig. 6(a)] the grain boundaries are invisible, passivated as they are from the *in-situ* hydrogenation. Figure 6(b) shows the LBIC-response for long wavelengths (1060 nm) for which the grain boundaries become visible again.



(a) Wavelength = 540 nm



(b) Wavelength = 1060 nm

Fig. 6. Laser beam induced current image of fabricated multicrystalline solar cell; short laser wavelength of 540 nm (a), and long wavelength of 1040 nm (b).

3. Cell process integration

The findings of the separate processing step optimisations have been combined in one process sequence. Figure 7 presents cross section of a screen printed solar cell fabricated in a process of firing-through PECVD SiN_x. The process consists of only six steps and includes only one wafer cleaning step and one high temperature step of shallow homogeneous emitter diffusion. The process flow is presented in Table 2. All processing steps can be directly implemented into mass production lines. There is also high throughput equipment available for each processing step. The efficiencies of 16.3% have been obtained from cells processed on 100 cm^2 multicrystalline substrates.

This process is perfectly suited for lower quality and defected multicrystalline materials like ribbons and electromagnetically casted multicrystalline (EMC) wafers bringing the absolute efficiency gain up to 2.5% over cells with TiO_x ARC layer. Table 3 shows enormous improvement in all cell parameters when a process of firing-through PECVD TiOx ARC is replaced by firing-through PECVD SiN_x.

Table 2. Sequence of the "firing through" screen printing process.

Step no.	Process description
1	Saw damage etching in alkaline (NaOH, KOH) solutions
2	Emitter diffusion (screen printing, spray-on, spin-on or from $POCl_3$)
3	Plasma etching of the edge parasitic junction
4	PECVD silicon nitride deposition
5	Front and rear contact screen printing and drying
6	Contact firing

Table 3. Characteristics of solar cells fabricated on defected multi-Si substrates (cell area 100 cm^2).

Process	J_{sc} (mA/cm^2)	V_{oc} (mV)	Eff. (%)
Firing-through APCVD TiO_x	23.7	569	10.3
Firing-through PECVD SiN_x	30.6	600	13.7

The further improvement of the cell parameters have been achieved when the firing through process had been combined with isotropic acid etching and/or selective single diffusion step selective emitter process described in sections 2.2 and 2.3. Although the firing through process has been developed for multicrystalline silicon substrates this process works also very well on Cz-Si solar cells bringing efficiency of screen printed solar cells near that obtained for industrial buried contact cells. Table 4 presents the summary of the best results for both types of substrates.

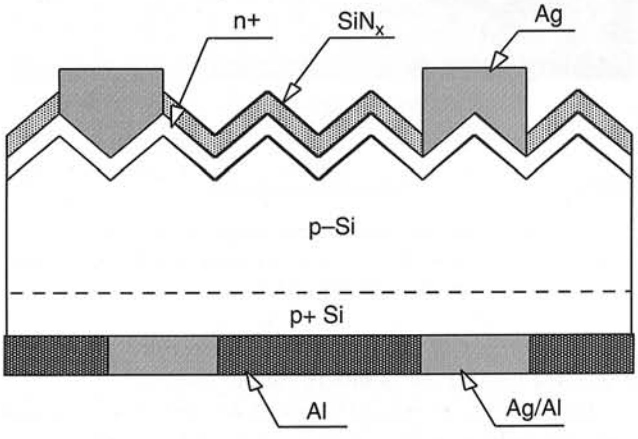


Fig. 7. Scheme of solar cell fabricated with firing-through PECVD SiNx process.

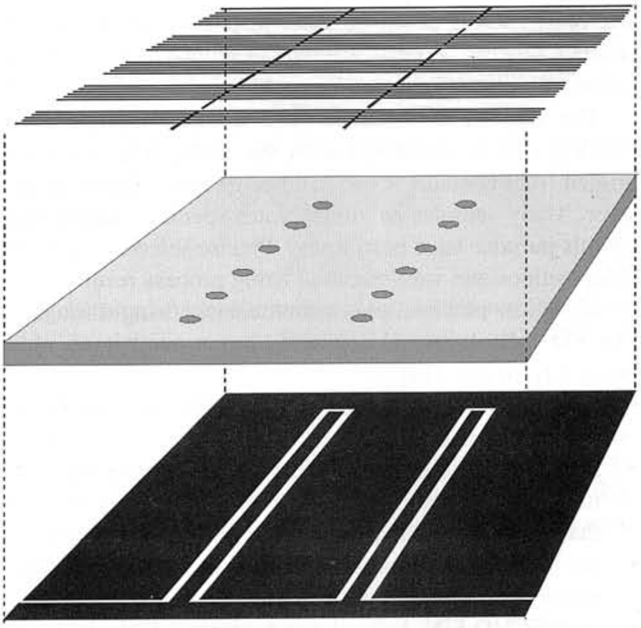


Fig. 8. Schematic representation of metallisation wrap through cell.

Table 4. Parameters of the best cells obtained on multicrystalline and monocrystalline silicon substrates. Cell area 100 cm^2.

Material and cell process	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff (%)
Multi-Si, isotexturisation, homogeneous emitter	34.8	614	77.4	16.5
Multi-Si, isotexturisation, selective emitter	34.6	625	77.6	16.8
Mono-Si, homogeneous emitter	35.4	619	77.7	17.3
Mono-Si, selective emitter	37.3	627	76.4	17.9

4. Back contact cell process

Close to one third of the total cost up to module manufacturing arises from the module fabrication itself. This implies that the reduction in module assembling costs can lead to significant overall cost reduction. One way to achieve this is to have both p and n contacts at the backside of the wafer. This allows a much higher degree of automation with less stringent handling restrictions on module assembly. Moreover, the shadowing losses are largely reduced on the front side. Various structures are given in the literature for back contact cells such as, the interdigitated back contact (IBC) solar cell [16], the front-surface-field solar cell [17], point contact solar cells [18], emitter wrap-through (EWT) cell [19] etc. For one-sun application with a cost-effective processing scheme a novel technology, called the metallisation wrap through (MWT) cell has been recently developed in IMEC [20], in where the busbars are moved to the backside of the cell with the fingers remaining on the front side and connected to the busbars via holes (Fig. 7). By this technology most of the difficulties encountered in applying the back contact technique to cost effective processes are overcome:

(a) since the p-n junction is close to the front surface the demand for material quality and surface passivation becomes less stringent,

(b) since the metal fingers are on the front side, only a small number of vias need to be made to contact the rear bus bar (a number of fingers can be grouped per via),

(c) the shadowing losses are still reduced because the busbars are moved to the rear surface,

(d) module connection becomes simple.

Initial WMT cells have been fabricated with full screen printing technology on 100 cm^2 multicrystalline Si substrates. A promising efficiency of 13.1% was obtained with Si_3N_4 ARC [20].

5. Summary

A simple industrial type process for high efficiency multicrystalline and monocrystalline solar cells has been developed. The number of processing steps has been reduced to six. All processing steps can be easily transferred to big volume production lines. Solar cells with average cell efficiency above 15% and 17% can be respectively obtained on large area multicrystalline and monocrystalline substrates. Including in the processing sequence the advanced processes of isotropic texturisation and selective emitter increases the cell efficiency to 16.9% and 17.9% respectively for multi- and monocrystalline silicon. A new cell concept metallisation wrap through cell, has been recently introduced. This cell structure aims at improvement of the visual appeal of cells and simplification of a module assembly process. The cell efficiency of 13.1% has been obtained in a simple cell processing sequence based on screen printed contacts.

Acknowledgements

This work has been in part financially supported by the Joule III Program of European Commission (DGXII) in the framework of the projects: JOR 3-CT-95-0011, JOR 3-CT-95-0030, JOR-CT-98-0226 and JOR-CT-98-0269.

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