Silicon surface texturing by reactive ion etching

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The high reflectivity of bare silicon substrates is reduced by roughening the surface with reactive ion etching (RIE). Silicon samples are immersed in a plasma chamber and ion assisted etching produces a high density of pits across the surface of the silicon. The obtained reflectivity is only slightly dependent on grain orientations and so RIE offers a way to effectively texture multi-crystalline substrates that cannot be easily textured using the methods commonly employed for single crystalline silicon. Typical reactive ion etching techniques produce a silicon surface with a very low reflectivity (black silicon). However, such surfaces increase carrier recombination and so the efficiency of the resulting solar cells is low. By adjusting the process conditions, the height and width of the surface features can be controlled to produce a surface that is sufficiently rough to couple light into the cell. Under specific conditions, etching pits are formed by intersections of {111}-crystallographic planes. The RIE selectivity for those planes causes a texture with {111}-surfaces and slows down the RIE process when this texture is formed. This effect causes a self-adjusting uniformity of texture over the whole substrate what might be of a use in batch reactors. Following the RIE process, short wet chemical etching removes the ion damaged silicon layer that is responsible for defect recombination of carriers. The etched surfaces are described using scanning electron microscopy and finished solar cells are characterised with spectral response.

Keywords: solar cell, texturisation, reflectivity, optimised structures.

1. Introduction

In order to improve the solar cell performances, incoming light on the cell has to be coupled into the cell and transformed into electrical energy more effectively. Losses due to reflection and transmission of the incident light have to be reduced to increase the solar cell efficiency. Reduction of surface reflectance is an efficient method to improve this efficiency. This reduction can be obtained by adding anti-reflection layers on top of the cell substrates as well as texturing the substrate itself. A texture causes a multiple reflection on its surface. Therefore, the amount of collected light into the substrate, depending on the amount reflections, increases. This increase of collection, together with the larger average path length of light in the substrate, causes an increased possibility of absorption.

There are several ways to obtain a texture on silicon substrates. Apart from structuring by masking and etching the substrate [1], there are cheaper and simpler ways of texturing which are more suitable, especially for the low cost production of multi-crystalline silicon (mc-Si) solar cells. A commonly used method is wet etching in NaOH or KOH solutions. This etch is selective for crystallographic orientations, and forms structures by the intersection of {111}-crystallographic planes in the silicon [2]. Because of random crystallographic surface orientations of grains in mc-Si, this texturing is optimal for only that part of the grains, which are close to the required (100)-orientation. Avoiding this grain dependency can be done by using an isotropic wet etch like several acidic solution [3–5]. This way of texturing relies on nucleation of etching on the surface of the Si substrate. Very smooth and flat substrates like EFG and dendritic web silicon ribbon crystals do have a lack of microscopic defects functioning as a nucleation point. Therefore those ribbon materials are difficult to texture chemically.

A texture can be applied to silicon substrates by a mechanical method also. But recent methods like V-grooving [6] and multi-wire sawing [7] still have to deal with a low throughput and low yield for fragile substrates. Especially ribbons are too thin and too breakable to apply mechanical texturing on.

Laser grooving is another non-reactive method for texturing substrates. The texture pattern is "written" by a laser in the substrate, which is not a fast process yet. This makes laser texturing a too slow process for high throughput industrial applications.

Another method of texturing, using reactive ion etching (RIE) has been introduced a few years ago [8]. RIE seems to be a method that overcomes all mentioned problems of texturing mc-Si substrates.

1.1. Reactive ion etching

Reactive ion etching is a kind of plasma etching, not only using the chemical etch ability of the plasma species, but also the kinetic energy of its ions. From the time plasma

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etching was applied in the semiconductor industry for patterning silicon substrates, it is known that plasma etching, under certain conditions, causes a surface texture of a very high roughness [9]. This texture is often called "silicon grass", by its very spiked structure; or "black silicon" by its large effect of light absorption. Reflectivity can be minimised to below 1% [10]. Decrease in reflectivity does not automatically lead to an improvement of cell efficiency. It is known that a less rough form of this texture can be used for more effective light coupling into silicon substrates [8,11]. The reflectivity can be well controlled by RIE. This way of texturing is ideal for very fragile substrates and is not grain dependent under certain etching conditions. The uniformity over the substrate depends strongly on the used RIE parameters which might be a big disadvantage for RIE batch reactors, needed for solar cell production.

The aim of this work was to find the RIE conditions that create a texture with a low reflectance, which obtains a maximum improvement for short circuit current, and with a good uniformity over the substrate.

2. Experiments

Silicon substrates were processed in an RIE reactor, suitable for dry etching of silicon. The first phase of experiments with RIE was performed to find an optimal texture, which would lead to a significant increase of the short circuit current I_{sc}. This first optimisation was done on 10×10 cm^2 mc-Si substrates. After RIE texturing, the substrates were processed to solar cells according a standard IMEC process flow (see Fig. 1), including emitter diffusion

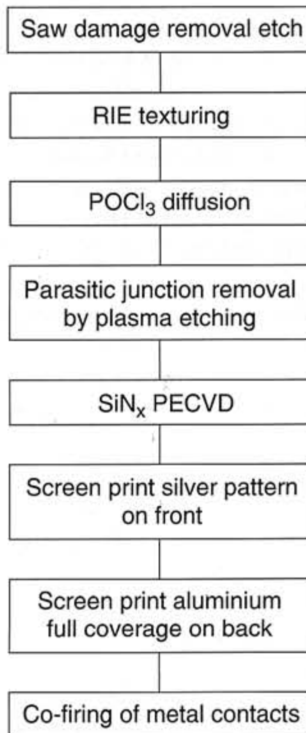

Fig. 1. Flow chart of the standard process at IMEC.

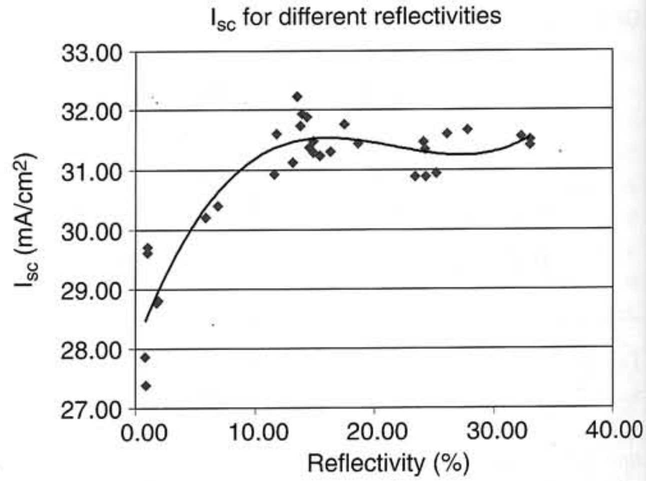

Fig. 2. I_{sc} of cells with different reflectivity, obtained from RIE texturing.

from $POCl_3$, passivation and anti-reflection coating from SiN_x PECVD. Reference cells, processed parallel to the textured cells, did not receive any texturing and were used to compare the contribution of the texture to the cell current. I-V curves and internal quantum efficiencies (IQE) were measured to investigate this contribution. Secondly, dimensions and the aspect ratio of the structures were investigated by scanning electron microscopy (SEM) to determine the RIE conditions for further optimisation. In this case, polished mono-crystalline wafers were used to investigate the precise form of the structure by atomic force microscopy (AFM) and SEM. The results from the tests on mono-crystalline substrates were confirmed by tests on multi-crystalline cells. Another set of experiments was done to solve problems like possible ion damage underneath the silicon surface that results in a higher recombination, affecting the open circuit voltage (V_{oc}).

3. Experimental results

By changing the conditions of the RIE process, it is possible to reduce the reflectivity to any value. For each set of textured wafers, a solar cell process has been executed. According to the I_{sc} measurements, it was found that a texture around a reflectivity of 15% should have an optimal contribution to the cell (Fig. 2). Cells with a reflectivity below

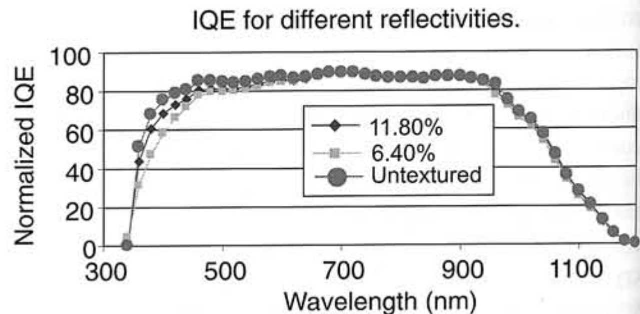

Fig. 3. Internal quantum efficiency of textured cells with low reflectivity, compared to reference cells with no texture.

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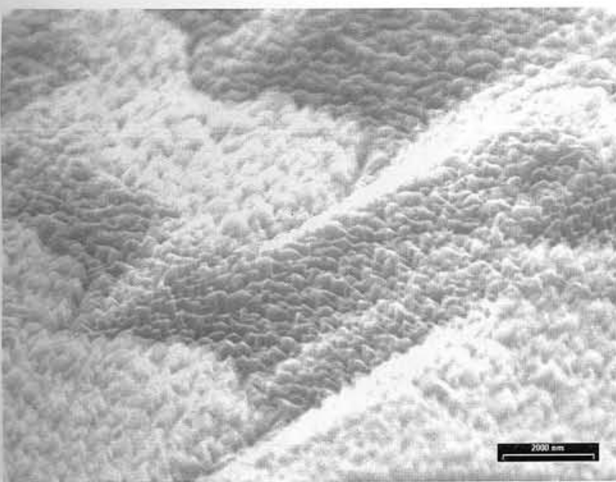
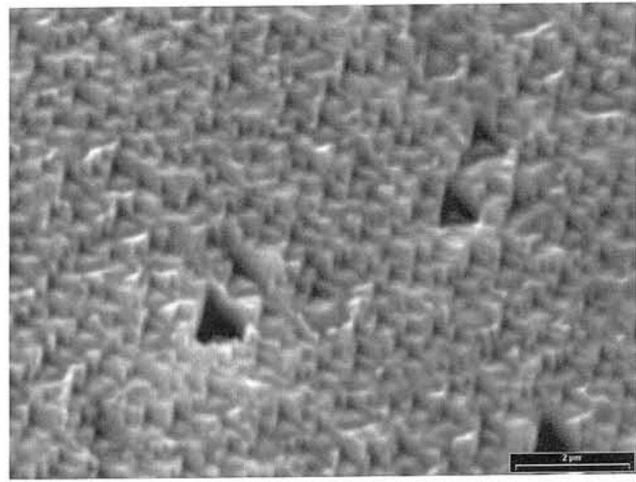
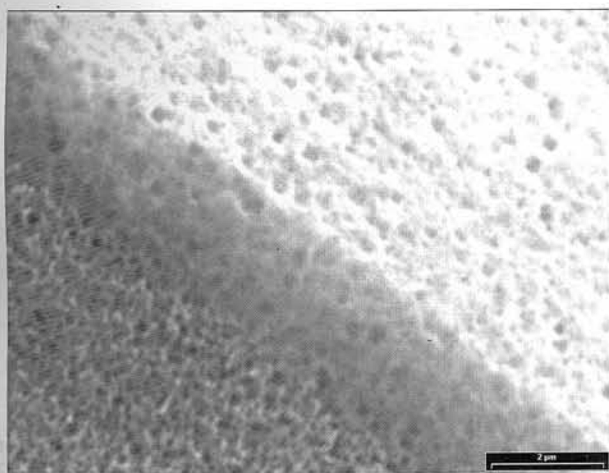


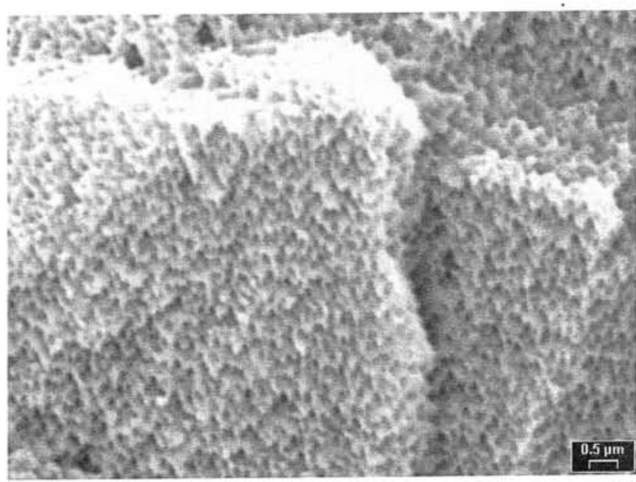
(a)



(b)



(c)



(d)

Fig. 4. SEM pictures of textures obtained by RIE processing: (a) uncontrolled texture on mc-Si with 15% reflectivity, (b) high density texture on polished (111)-mono-Si, (c) grain depending structure of uncontrolled texture, (d) (111)-orientated surfaces of textured mc-Si.

15% have a low I_{sc} due to a lower IQE in the short wavelength region, as presented in Fig. 3.

Printing a silver paste front contact on a heavy textured cell is problematic. A bad contact of the silver paste with the texture causes deformation of the lines after annealing steps as drying and firing. This causes peeling of the contact lines and results into high series resistance. Textures, giving a reflectivity above approximately 10% doesn't show this problem. In many cases, the uniformity of the texture becomes worse with the increase of reflectivity. Also the difference of reflectivity and textures between the grains can be large [see Fig. 4(c)].

The mechanism of RIE texturing seems to be dependent on the crystallographic orientation. Differently orientated surfaces need different minimal ion energies to get broken by a chemical-kinetic ion reaction. Process conditions as ion current, rf power and pressure have a direct influence on the ion energy, thereby they control the etch anisotropy. Under certain conditions, the RIE starts to become more selective for different crystallographic planes. This results in pits on the surface with intersection of {111}-planes. Pyramid-like and tetrahedral pits are formed. If the density of the pits is high enough, surfaces with a controlled structure or facets are formed [see Fig. 4(b)].

It is observed that texturing process is influenced by the deposition of etch residue on the reactor chamber walls as well as on the substrate. One result of this effect is the local formation of an absorbing layer on substrates. It is hard to make a good emitter on those layers. The layer is very black, but rather flat. According to SEM observations, the layer seems to exist of kind of amorphous silicon, formed by reactions with silicon-halogen molecules. Figure 5 and other SEM pictures reveals that this layer seems to be re-deposited and covering the surface structures.

Another problem is the ion-induced damage at the surface. According to literature this damage can be heavily from 10 to 50 nm deep and causes a low V_{oc} due to the defect recombination of carriers [12]. A slow wet etching has to remove the damaged layer without etching the texture off. This etching can be well controlled for surfaces with

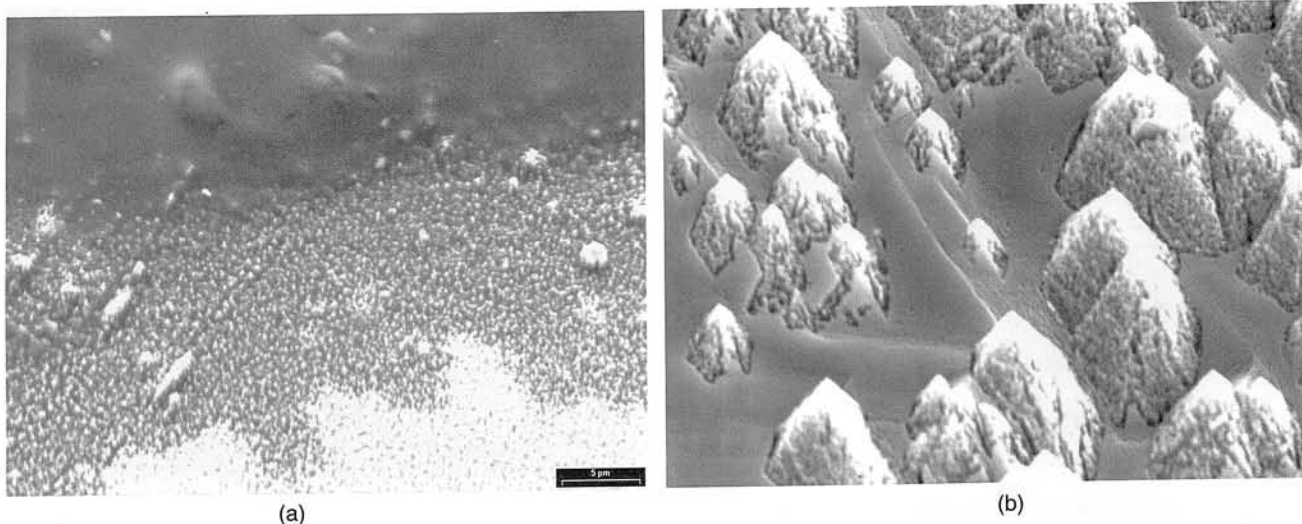


Fig. 5. SEM pictures of dark regions: (a) amorphous silicon coverage on monocrystalline silicon, (b) amorphous silicon on mc-Si substrate.

Table 1. Electrical results of RIE textured cells.

Substrate	Wet etch time	Reflectivity after wet etch	I_{sc} (mA/cm^2)	V_{oc} (mV)
Reference		No texture	30.8	614.4
RIE		19.4	31.6	603.3
RIE	1	19.6	31.6	608.0
RIE	3	21.9	32.2	611.8

{111}-facets in diluted etch solutions. Those surfaces etch much slower than uncontrolled textured surfaces as results in Fig. 6 show. Different etchings were performed on different RIE textured mc-Si substrates with a similar reflection. Average electrical results of the completed solar cell are presented in Table1 and show a recovery of V_{oc} to nearly the value of untextured cells. Etching preserved the shape of the structure, so the reflectivity was hardly changed.

A reduced reflection resulted in increase of the I_{sc}. For the etched cells the I_{sc} increased with average 1.4 mA/cm^2 compared to the reference cells.

4. Summary

Reflectivity can be varied to any value below those of untextured substrates by changing the RIE process conditions. With the decrease of reflectivity, the cell current

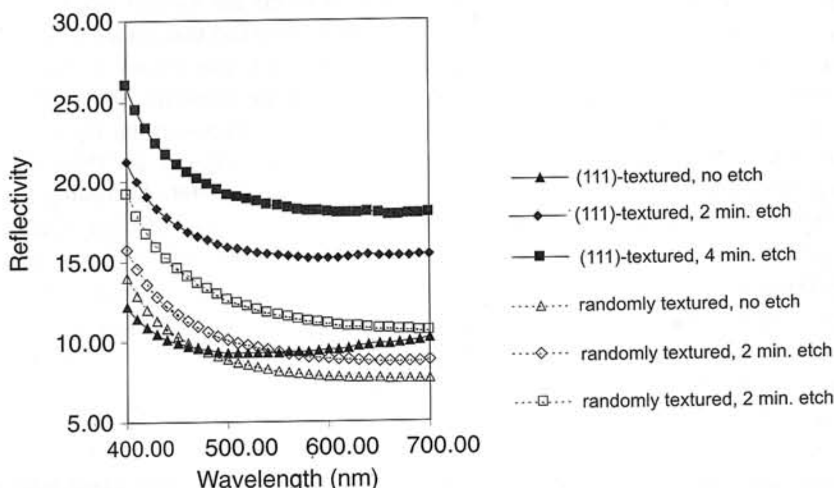


Fig. 6. Reflections of {111}- and uncontrolled textured substrates at different wet etch times.

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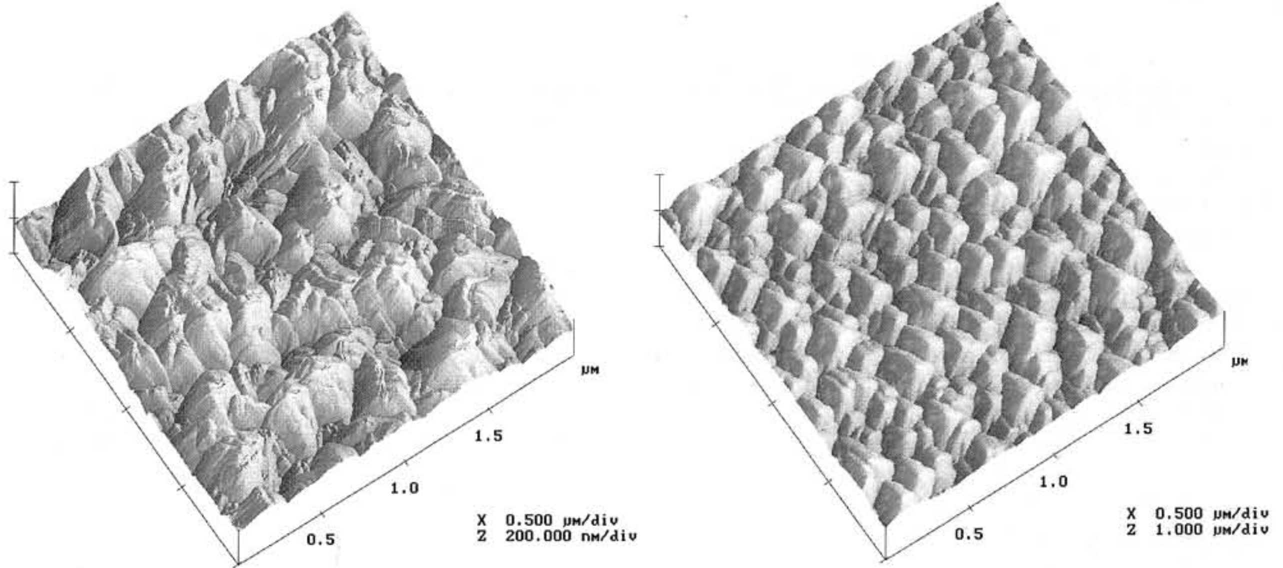

Fig. 7. AFM scans of surface texture, obtained by different RIE conditions.

rises. But not when the reflectivity is very low. At very low reflectivity, the texture has an uncontrolled needle-like form. This causes an inhomogeneous junction depth after emitter diffusion. Due to the small width the peaks will be totally diffused. A part of the transmitted light will be absorbed at the surface of the top of the peaks instead of contributing to the cell current. This is especially true for the short wavelength regime as the results from the IQE in Fig. 3 shows. An optimal reflectivity was found at 15%. However, the texture itself still can be optimised. The I_{sc} improves when the substrate is textured with facets with {111}-surfaces instead of an uncontrolled texture. A texture of {111}-facets can be applied on every crystallographic surface orientation, even on polished (111)-Si wafers [see Fig. 4(b)]. Dimensions of the {111}-facets can be changed by adjusting the RIE conditions (see Fig. 7). A large advantage of these formed {111}-facets is its self--stopping etching process, which obtains a uniform textured surface over the whole substrate. It is observed from the glow discharge radiation that the RIE stops, or slows down when the {111}-facets are formed. This means that any non-uniformity of texture will be removed when etching will last long enough. Areas on the substrates, which are textured, will not etch further, while areas that are textured slower will proceed, until {111}-facets are formed there. This implies that a batch RIE reactor with a large total surface of loaded substrates will texture with a self-adjusting uniformity. A difficult and complex modelling of plasma division and gas streams might be unnecessary.

It is observed that {111}-facets are etching slower in wet chemicals than uncontrolled textured surfaces. Therefore {111}-facets are easier to control in removal of a small ion damaged top layer in etch solutions of a realistic small dilution. This method is an easy treatment to restore V_{oc}. At least it is an easier approach than modifying the RIE process conditions, what might limit the freedom to control the dimensions of the texture. This freedom to control the texture is important to obtain the right aspect ratio and density, in order to optimise the reflection and the emitter profile.

Another problem might be the amorphous silicon, formed by some halogen-silicon residues. This formation seems to be depending on the process settings and on the amount of residues, built up from former runs. Since this amorphous silicon is not formed on all substrates and for all process conditions, this problem does not seem to be very important and can be avoided by a better control of residue deposition in the chamber.

5. Conclusions

Substrates for silicon solar cells can be textured by RIE for decreasing reflectivity to gain higher short circuit current. An optimal reflectivity for uncontrolled textured cells was around 15%. Structures with lower reflectivity give problems in emitter diffusion and metal contact screen print. On substrates with larger structures, an emitter that follows the surface structure can be better applied. This means that aspect ratio, and thus the reflectivity, can be decreased below 15% without current decrease.

Current increase is obtained by texturing substrates with optimised structures. Those structures consist of facets with {111}-surfaces. The formation of {111}-facets is also of use to get ion damage removal by wet etching controllable. One effort of this texture is that it can be applied on any crystallographic surface orientation and is not dependent on those orientations of grains in mc-Si. The dimensions and thus the reflectivity as well, can be controlled by process parameters. Another advance of {111}-facet textures is the self-stopping effect of RIE. The uniformity of texture will be improved by this self-stopping RIE. This self-adjustment of uniformity can be very useful in RIE batch reactors.

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