OPTO-ELECTRONICS REVIEW **8**(4), 375–377 (2000)

Electrical characterisation of CdTe/CdS photovoltaic devices

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Thin film solar cells based on CdTe/CdS are expected to become the base material for the low-cost and efficient large-scale solar energy conversion devices. The samples have been investigated using current-voltage (I–V) and capacitance-voltage (C–V) measurements in order to define the transport mechanism in heterostructure and basic electronic parameters. Trap-assisted tunnelling has been found to dominate carrier transport mechanism in the junction.

Keywords: CdTe, current-voltage characteristics, capacitance.

1. Introduction

Thin film CdS/CdTe heterojunction solar cells are one of the most promising photovoltaic devices for the low-cost large-area terrestrial applications [1]. CdTe has an energy gap of 1.45 eV, very well suited to absorb the solar light spectrum. Therefore the absorber layer needs to be only a few μm thick to absorb > 90% of light above the band gap.

Several groups have studied solar cells based on CdTe/CdS prepared by means of different techniques [2–4]. Fabrication differences cause various device properties. This is probably also a reason of differences in characteristics and models presented by them.

Investigation of junction transport in these devices is essential for understanding the photovoltaic loss mechanism and achieving higher efficiency. In this work solar cells based on CdTe/CdS have been characterised using I–V and C–V measurements in order to define the transport mechanism in heterostructure, basic parameters, and the junction structure.

2. Experimental

The devices investigated in this paper have been prepared in ETH-Zurich [5]. Glass as a transparent substrate and FTO layer as transparent conducting electrode have been used. This oxide has the energy gap between 3 and 3.4 eV, depending on deposition processes. CdS and CdTe films have been grown in ultra high vacuum chamber and annealed at 450°C. After $CdCl_2$ treatment and annealing at 430°C, the CdTe surface has been etched using a Br-methanol solution. It is well known that a $CdCl_2$ treatment of the CdTe/CdS layer causes a recrystallisation and improves the solar cell efficiency. The deposition of the Cu/Au back electrode and short annealing at 300°C have been the last steps.

The photovoltaic parameters for a typical sample, measured with illumination intensity 75 mW/cm^2, are the following: the open-circuit voltage V_{oc} of about 820 mV, the short-circuit current I_{sc} = 17.3 mA/cm^2, the fill factor FF is 57%, and the efficiency η = 10.5%. The area of the sample equals 0.125 cm^2.

I–V and C–V measurements have been performed in a cryostat in the temperature range of 130–360 K. For the C–V measurements a capacitance bridge DLS-82E has been used.

3. Results

3.1. C–V characteristics

A slop of Mott-Schottky plot $1/C^2$ as a function of voltage reverse bias should yield a net concentration of shallow acceptors. However, two curves measured with a different direction of voltage sweep formed hysteresis are shown in Fig. 1. We attribute this hysteresis to a large concentration of deep traps. The concentration of midgap traps distorting the C-V profile is at least of the order of the net shallow acceptor concentration. Applying the reverse bias causes emptying of deep traps and then we get a true concentration of shallow acceptors. The doping concentration obtained for various samples is in the range of $(2–5)\times10^{14}$ cm^{-3} and the main diode barrier height E_b is of about 1.4 eV.

We conclude that C-V characteristics should be measured after applying reverse bias for several minutes at room temperature in order to obtain the true profile of shallow acceptors.

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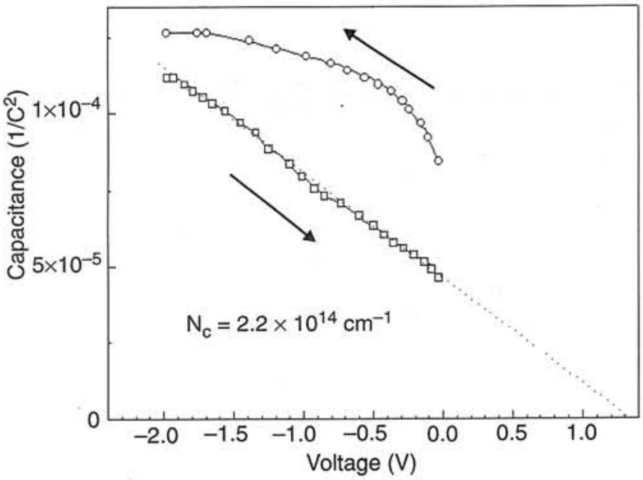

Fig. 1. Mott-Schottky plot obtained at room temperature for two directions of voltage bias sweep.

3.2. I–V characteristics

Typical I–V curves have been shown in Fig. 2. The I–V characteristics have been measured in dark at the temperature range of 134–330 K with the step of about 20 K. The forward-bias segment up to 0.8 V of the I–V characteristics has been modelled by the following equation

$$I = I_0\{\exp(V/nkT) - 1\} + V/R_{sh}$$

where R_{sh} is the shunt resistance, n is the ideality factor and $I_0 = I_{00}\exp(-E_a/kT)$. The activation energy of saturation current is related to the barrier height by $E_a = E_b/n$.

The ideality factor n depends on temperature as shown in Fig. 3. At room temperature n equals about 1.5, for lower temperatures n is higher than 2. That suggests a trap-assisted tunnelling to interface states to be the dominating transport mechanism, at least below room temperature [6]. It has been shown by the use of DLTS that concentration of midgap states in CdTe/CdS is high [7], which supports that conclusion.

Figure 4 shows the dependence of I_0 vs. inverse temperature for various samples. The activation energies E_a obtained at temperatures close to room temperature are in the range of 0.4–0.8 eV. Values are much lower than expected, because the tunnelling of carriers to interface lowers the effective barrier height.

For higher forward voltage, current limiting effect appears due to a back contact. We attribute the saturation of the current in the forward direction to a back contact barrier V_{bc}. In Fig. 5 the back diode saturation current I_b has been plotted as a function of inverse temperature. Hence, we obtain a value of the back contact barrier V_{bc}. For the investigated samples V_{bc} is in the range of 0.31–0.33 eV. A similar value has been reported by McCadless *et al.* [8] and has been attributed to a junction between CdTe and copper tellurides detected at the contact surface.

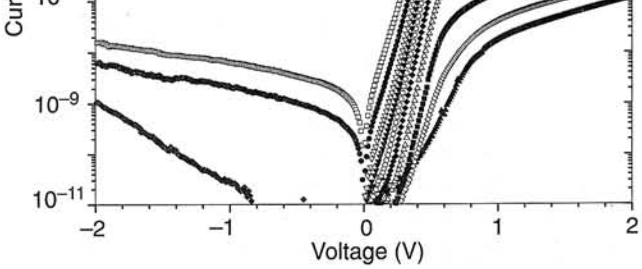

Fig. 2. Current-voltage characteristics for a representative sample.

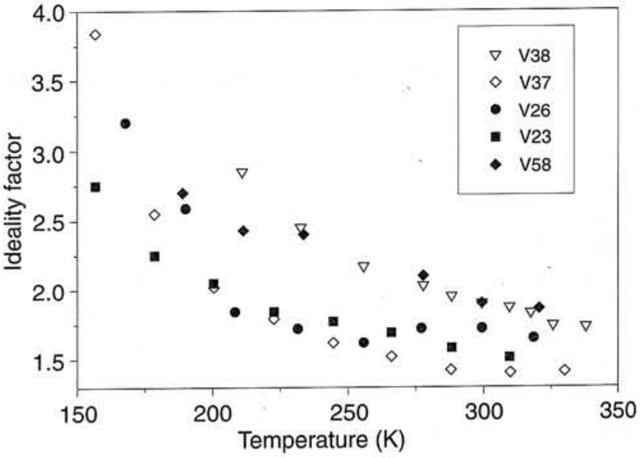

Fig. 3. Ideality factor as a function of temperature for several samples.

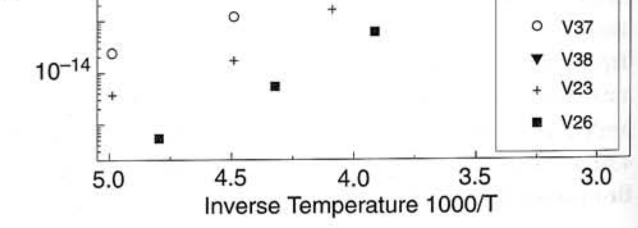

Fig. 4. Saturation current of a main diode as a function of inverse temperature for several samples.

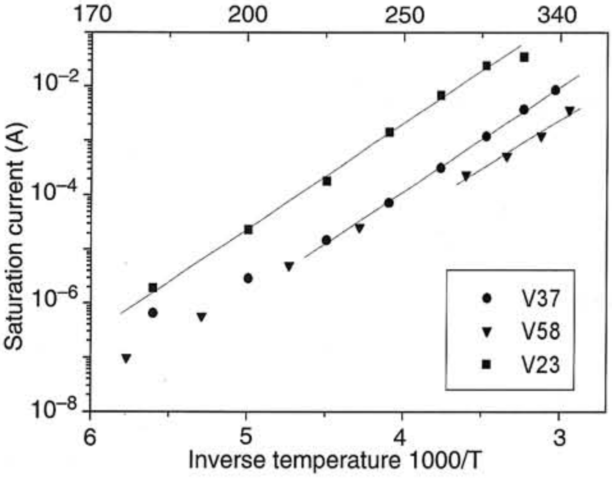

Fig. 5. Saturation current of a back diode for high forward bias as a function of inverse temperature, for several samples.

4. Conclusions

We have shown that the trap-assisted tunnelling to interface levels is the dominating electron transport mechanism in CdTe/CdS solar cells in the forward-bias region. It decreases the effective barrier height and thus enhances interface recombination. We conclude that relatively low fill factors and open-circuit voltages typical for the investigated samples are mainly caused by the high probability of tunnelling of holes to interface. The back contact barrier of the height of about 0.3 eV is not a factor, which limits the photovoltaic performance [9]. Figure 6 shows a proposed energy band model for the CdS/CdTe heterostructure. The concentration of midgap traps taking part in the tunnelling and distorting the C–V profile is at least of the order of the net shallow acceptor concentration. The doping concentration obtained from C–V characteristics is in the range of $(2–5)\times10^{14}$ cm^{-3}.

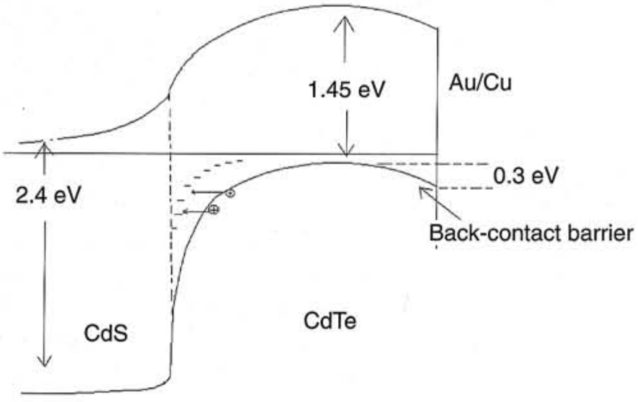

Fig. 6. Band model for a CdS/CdTe solar cell with a second barrier at the back contact and with trap-assisted tunnelling of holes to interface levels shown.

Acknowledgements

This work has been supported by Swiss National Science Foundation under the Institute Partnership programme.

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