Contributed paper

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HgCdTe MBE grown LWIR linear arrays

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Mercury-cadmium-telluride (MCT) 2×64 linear arrays with silicon readouts were designed, manufactured and tested. MCT layers were grown by MBE method on (103) GaAs substrates with CdZnTe buffer layers. 50×50 μm n-p-type photodiodes were formed by boron implantation.

The parameters of long wavelenght infrared MCT linear arrays with cutoff wavelength $\lambda_{co} \approx 10.0$–$12.2$ μm and Si readouts were tested separately before hybridisation. The HgCdTe arrays and Si readouts were hybridised by cold welding In bumps technology.

Dark carrier transport mechanisms in these diodes were calculated and compared with experimental data. Two major current mechanisms were included into the current balance equations: trap-assisted tunnelling and Shockley-Reed-Hall generation-recombination processes via a defect trap level in the gap. Other current mechanisms (band-to-band tunnelling, bulk diffusion) were taken into account as additive contributions. Tunnelling rate characteristics were calculated within $k \cdot p$ approximation with the constant barrier electric field. Good agreement with experimental data was obtained.

Keywords: MCT linear arrays, silicon CCD readouts, tunnelling.

1. Introduction

High performance infrared (IR) imaging systems basically include focal plane arrays (FPAs) with multielement scanning linear or starring two-dimensional arrays of photovoltaic (PV) detectors cooled down to cryogenic temperatures with a signal processor in the focal plane. The FPA technologies mainly include two major technologies, hybrid and monolithic. The concept of IR FPA hybrid technology is widespread and permits the optimisation of separate parameters of the detector array, which has a large number of sensitive elements, and typically silicon readout device coupled with detector array [1]. The major hybrid technology uses MCT PV detector chips and silicon CCD or CMOS chips [1,2] for readout and multiplexing the sensed charge from the detectors.

At present, the use of MCT based FPA detectors for IR imaging applications in 8–12 μm and also in 3–5 μm wavelength bands is well justified. Medium-and long-wavelength infrared HgCdTe photodiodes and arrays have the most suitable parameters for IR technology applications [3–5]. Because the input transistors of the read-out devices of the hybrid array should be reverse biased [6], the photodiodes connected with them via, e.g., In bumps, are reverse biased too. Thus, to optimise the array operation, it is important to ground the value of bias at which the array can operate most effectively as the carrier transport mechanisms are changing in the depletion region on bias value, and the diodes parameters can change essentially on bias in dependence on the mechanism of carrier recombination in and near depletion region.

To have high quality HgCdTe homogeneous layers to manufacture PV detectors with substantial yield, it is important to grow them for these purposes by good established methods on large square substrates. Here an MBE procedure was used to grow large area MCT layers on GaAs 3-inch (103) substrates with an intermediate CdZnTe layer.

2. Growth procedure and properties of the layers

MCT MBE growth technology on gallium arsenide wafers was used with an intermediate CdZnTe layer. The advantages of the MBE technology are at creating the epitaxial layers and seem to be the most adaptable for production of large area MCT arrays.

MCT epitaxial layers were grown on 3-inch diameter (103) GaAs substrates with an intermediate CdZnTe buffer layer. The growth temperature was within T = 180–190°C for HgCdTe layers and within T = 240–300°C for CdZnTe buffer layers. During the growth process the layer compositions were controlled by a built-in ellipsometer. The non-uniformity of the composition over an area of 1 cm^2 was not more than $\Delta x = \pm 0.001$. The as-grown layers were of n-type conductivity and should be converted to p-type conductivity to use boron implantation for receiving n-p diodes to be used with n-channel CCD readouts.

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After 200 hours of annealing at T ≈230°C, the as-grown HgCdTe layers of n-type conductivity were converted to p-type conductivity layers. In the annealed samples the hole concentration P and the mobility μ_p values in the film bulk at T = 77 K were about $P_{77} \approx 6\times10^{14}$ cm^{-3} and $\mu_{77} \approx 320$ cm^2/V×sec, respectively.

To decrease the influence of surface recombination of the HgCdTe layers, they were grown with increased surface composition of x value [7]. The sample has special wide gap regions of d ≈ 0.5 μm thick with composition x ≈ 0.55 near the surface, while in the layers the composition value was within x = 0.219–0.220.

The epitaxial MCT layers on $Cd_{1-y}Zn_eTe$ (y ≈ 0.04) buffer layers are lattice-matched, and have sufficiently high crystal perfection, which is mainly determined by the substrate quality, allowing the possibility to design IR arrays operating in the BLIP regime. Using gallium arsenide or silicon substrates the growth of a large area of rather high quality MCT epitaxial layers is possible [8]. Still, the structural perfection of these layers is poorer than the analogous ones on CdZnTe single crystal substrates. Nevertheless, MBE grown on alternative to CdZnTe substrates are suitable for manufacturing large area arrays for the 8–12 μm wavelength region.

The limiting process of surface at MCT layers MBE growth procedure is the dissociation process of diatomic Te molecules [8]. Dissociation is favoured at the surfaces with high step densities and this is the reason why for MCT layers growth technology on the alternative substrates orientations (112) or (013) are used. Dissociation is favoured when absorbed Te_2 molecules are surrounded by metal atoms. At low temperature growth at high densities of Hg atoms absorbed at the surface with high step densities, the growth of layers near to normal one can be realised, and it is possible to obtain the most smoothest MCT surfaces.

At temperature growth the density of absorbed at the surface Hg atoms is decreased and, accordingly is lowered the fraction of surface where dissociation of Te_2 molecules takes place. At high temperatures dissociation of Te_2 molecules will take place only at some points of the surface, where enough Hg atoms are situated and these are points with certain brakes at the steps. In such points the growth will be preferable. At higher temperatures the normal growth will be complicated and material precipitation will take place at surface points with certain steps and brakes configuration. Relief form the parts of crystallographic planes with minimal growth rate will be formed. This means that the temperature increase will lead to relief formation. This is confirmed by the analysis of surface relief by Atomic Force Microscopy (AFM) (see Fig. 1).

At lower temperature (T = 172°C) there is seen a gentle relief (Fig. 1.1). At higher temperature (T = 185°C) a well-ordered wave relief is distinctly observed (Fig. 1.2). Temperature on surfaces during the growth procedure was measured by special optical pyrometer. Temperature growth decrease the density of absorbed layer of the elements of the second group and decrease at the same time the probability of appearance of sections with successful for MCT layer growth configuration. Ordered relief at high temperatures is not the consequence of the steps order. Though (013) surface consists of steps, but layered growth and echelon of steps formation can not be realised at these temperatures, because of strongly absorbed diatomic Te molecules plays a role of impurity which blocks the growth (decreases kinetic coefficient at the step). Relief ordering than can be an evidence of collective character of the MCT processes surface crystallisation.

The as-grown MCT layers have electron concentration of 10^{14}–10^{15} cm^{-3}. This can be the reason of antisite Te [9], interstitial metal atoms [10], vacancies in telluride sublattice [10], and impurity atoms, first of all in this case gallium, when GaAs substrates are used. It is an important to ascertain a nature of n-type conductivity and electron concentration value of MBE as-grown MCT layers at temperature T ≈180°C. The results of calculations of antisite Te equilibrium concentration have shown that equilibrium concentration of antisite Te ($N_{Te} \approx 10^7$–10^8 cm^{-3}, calculated enthalpies of antisite Te in CdTe and HgTe are equal accordingly $\Delta H_{Te(Cd)}$ = 58.05 kcal/mol and $\Delta H_{Te(Hg)}$ = 20.50 kcal/mol) is too small (several orders less) at these

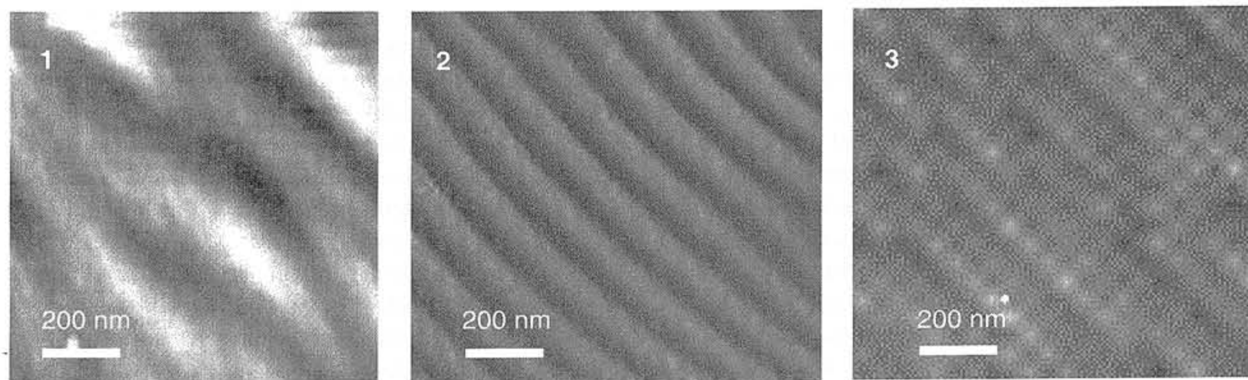

Fig. 1. MCT layers AFM images at different temperatures: 1 – T = 172°C (period l ≈ 2500 Å, surface irregularities h ≈ 10 Å), 2 – T = 185°C (period l ≈ 1700 Å, surface irregularities h ≈ 50 Å), 3- image (phase contrast regime) of the surface part, which is periodical in two directions (period l ≈ 1100 Å).

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temperatures to explain the electron concentration of $N \approx 10^{15}$–10^{16} cm^{-3}.

Another reason of this value of phone electron concentration may be the influence of Ga doping when GaAs substrates are used. The results of electrically active Ga concentration calculations at equilibrium conditions are shown in Fig. 2 for MCT layers with different Hg content. As one can see from Fig. 2, Ga solubility at growth temperatures of MBE method is too low ($N_{Ga} \approx 10^8$–10^{10} cm^{-3}) and cannot explain observable phone electron concentrations. At growth temperatures typical, e.g., for LPE or VPE methods (T ≈ 450°C) Ga solubility increases to $N_{Ga} \sim 10^{16}$–10^{17} cm^{-3} and it can lead to increase of electron concentration in the layers grown on GaAs substrates. It seems that Ga cannot be a primary donor impurity in MBE grown on GaAs substrates MCT layers, as, e.g., for such layers grown on (112) silicon substrates the phone electron concentration is the same order as for layers grown on GaAs substrates.

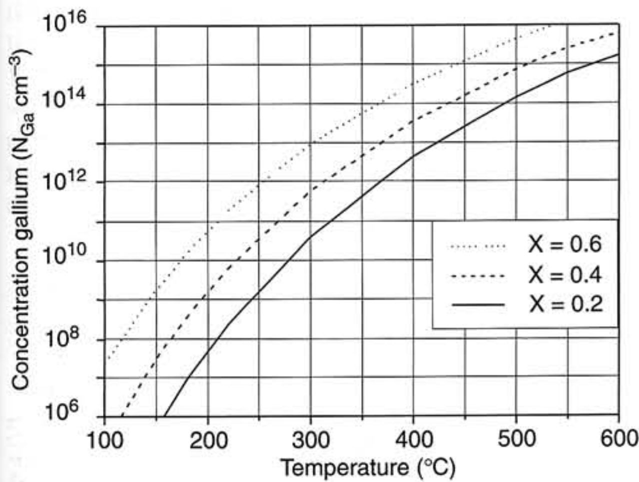

Fig. 2. Temperature dependence of electrically active Ga in MCT layers with different Hg content, calculated in equilibrium approximation for Te activity Q=1.

Electron concentrations observed in MCT layers can be explained by antisite non-equilibrium Te capture model. Ordinary defect transfer from surface to bulk leads to increase of free energy and thus defect equilibrium concentration in the bulk is higher compared to the surface one. At small or zero supersaturation conditions in the growing layers there will be inserted defects with almost equilibrium concentrations because there is no driving force to include defects above equilibrium concentrations. But, the layer growth takes place at some supersaturation ΔG_{ss} which in MBE methods can be substantial. Supersaturation conditions increase the probability of the defect formation configurations in the layers proportionally to $\exp(\Delta G_d - \Delta G_{ss}/RT)$, where R is an universal gas constant and ΔG_d is defect Gibbs potential. With temperature increase a supersaturation decrease and there should be a decrease of antisite Te concentration which is donor type defect in MCT layers, as it is shown in Fig. 3.

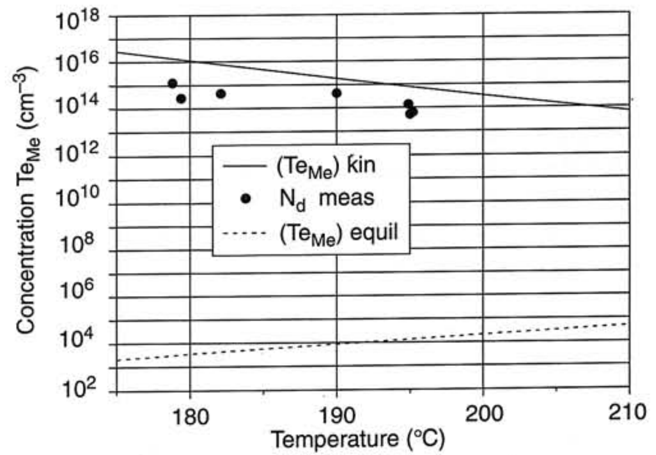

Fig. 3. Antisite Te concentration temperature dependencies in $Hg_{0.8}Cd_{0.2}Te$ MBE grown layers for equilibrium conditions (dotted line) and in the case of non-equilibrium capture in supersaturation conditions (solid line). Points are electron concentration data.

Here also are shown the measured electron concentrations in as-grown MCT layers for some growth temperatures. One can see qualitative agreement between the tendencies of non-equilibrium Te capture data and electron concentrations in MCT layers. A ΔG supersaturation value was estimated from the components partial pressure values used in experiments. As one can see a non-equilibrium antisite Te mechanisms of doping is opposite in temperature dependence to an equilibrium one.

One of the most important parameters of MCT layers is the composition uniformity across the film area. For an FPA operating in the 8–12 µm spectral range, the changes in composition should not exceed the value Δx = 0.001 across the array area, which for, e.g., a 256×256 array with pitch of about 40 µm, is about 10 mm. To provide uniformity in composition and thickness uniformity of epitaxial MCT layers across the wafer diameter, special molecular sources were designed with practically constant (during long-time processes) molecular flows. By knowing the changes in flow caused by decreasing the materials in crucibles, it was possible to correct the temperature of the source to maintain stable molecular flows.

2. Diode properties

In MBE grown and annealed p-type HgCdTe MBE epitaxial layers 264 focal plane arrays with 100-µm pitch and 50×50 µm n-p-type photodiodes were manufactured by low temperature planar technology. The photodiodes were obtained by boron implantation with particle energies E ≈ 80–120 keV.

Dark currents at V ≈100 mV reverse biases in diodes chosen for hybridisation in the arrays with λ_{co} = 10.5–12.2 µm as a rule did not exceed the values of I = 5–30 nA, and their zero-bias resistance-area product was within $R_0A \approx 20$–30 Ω cm^2 in dependence of λ_{co}. The aver-

age R_0A values for array elements within one of the wafer with $\lambda_{co} = 12.2$ μm were $R_0A \approx 6\ \Omega\,cm^2$.

Before hybridisation with CCD multiplexers, the current-voltage characteristics of photodiode arrays and their dynamic resistance versus bias voltages were measured. The typical results are given in Fig. 4 for one of the diodes in the array. One can see that even for rather low values, compared to those of diodes with $\lambda_{co} = 10$ μm, the values of dynamic resistance R shown at a reverse bias of 60–100 mV, are sufficient to operate with direct injection input circuits of CCD readouts.

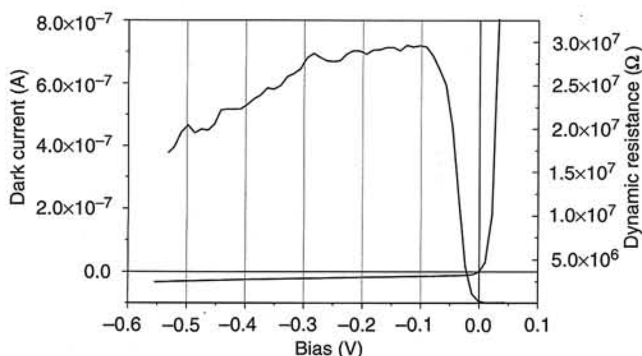

Fig. 4. Dark current and dynamic resistance vs bias voltage of typical MCT diode (x = 0.21). $R_0A \approx 6\ \Omega\,cm^2$.

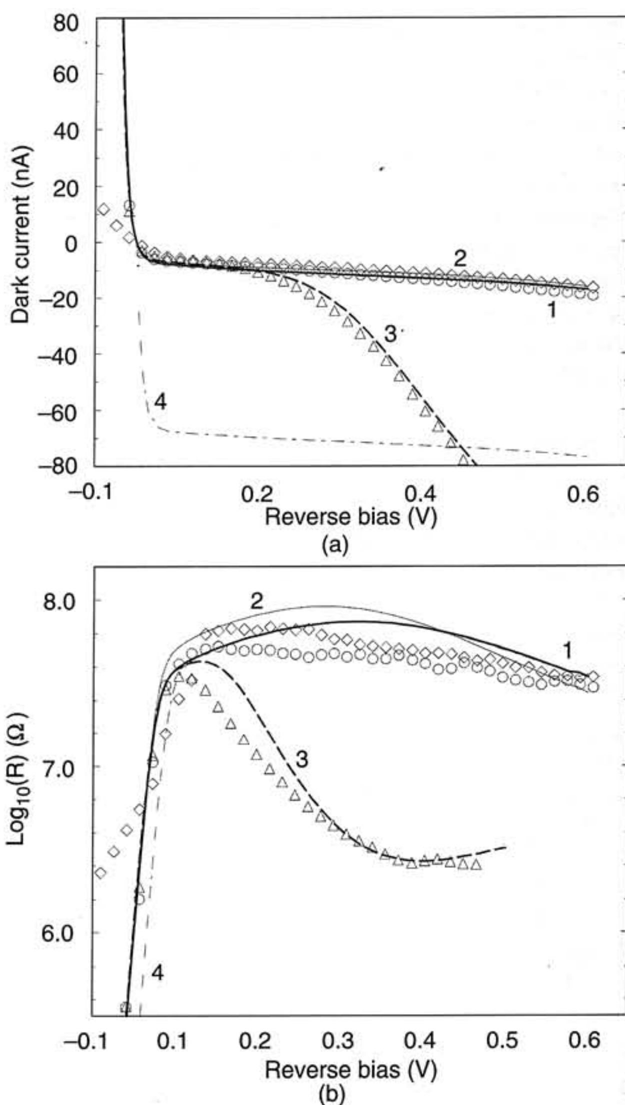

Fig. 5. Experimental and calculated current-voltage (a) and resistance-voltage (b) characteristics for some $Hg_{1-x}Cd_xTe$ (x = 0.212) diodes, T = 77 K. Curves 1: circles are experimental data, solid lines are calculated data with parameters: $E_t = 0.6\ E_g$, $N_d = 10^{15}\ cm^{-3}$, $N_a = 3\times10^{16}\ cm^{-3}$, $N_t = 2\times10^{13}\ cm^{-3}$, $N_{tbulk} = 2\times10^{13}\ cm^{-3}$, $\tau_{n,p} = 3\times10^{-7}$ s, $\tau_{bulk} = 6\times10^{-6}$ s, $E_g = 0.1016$ eV. Curves 2: diamonds are experimental data, thin solid lines are calculated data with parameters: $N_t = 3\times10^{13}\ cm^{-3}$, $\tau_{n,p} = 4\times10^{-7}$ s, all rest parameters are similar as for curve 1. Curves 3: triangles are experimental data, dotted line are calculated data: $N_{tbulk} = 6\times10^{14}\ cm^{-3}$, $N_t = 6\times10^{15}\ cm^{-3}$, $\tau_{n,p} = 3\times10^{-7}$ s, $\tau_{bulk} = 8\times10^{-6}$ s, all rest parameters are similar as for curve 1. Curve 4: chain line is calculated data for inverted p^+-n-structure. $N_a = 1\times10^{15}\ cm^{-3}$, $N_d = 3\times10^{16}\ cm^{-3}$.

Here some properties of MCT photodiodes with different I–V and R–V characteristics for spectral region of 8–12 μm were analysed.

The current balance equations approach taking into account two major current mechanisms, namely the trap-assisted tunnelling (TAT) and Shockley-Reed-Hall (SRH) generation-recombination processes was used [12]. Other current mechanisms (band-to-band tunnelling, bulk diffusion) were taken into account as additive contributions. Using donor and acceptor concentrations, trap level concentrations, trap level energy, and in-junction trap level lifetimes as fitting parameters, a reasonable agreement with the experimental data was obtained. To obtain the total non-equilibrium recombination rate the following two approximations were also used here: (i) the constant field barrier potential, and (ii) constant quasi-Fermi level across the barrier (this latter assumption is valid for forward or small reverse biases).

It was shown that the balance equation approach, taking into account two main current mechanisms (TAT and SRH) allows one to describe reasonably well the experimental data for MCT photodetectors (see Fig. 5) in their operational voltage range (most of input transistors of readouts operate at reverse biases $V_R \leq 0.1$ V). In all cases with diodes parameters investigated it was obtained (as a result of the fitting procedure) that the trap concentration $N_t \approx 10^{15}$–$10^{16}\ cm^{-3}$ is comparable to donor and acceptor concentrations. That is because it was taken into account the balance between TAT and SRH processes. If they are taken into account independently it can be resulted in too low concentration of traps. Such approximation used according e.g., to Refs. 13 and 14 gave unreasonably low concentrations of tunnelling centres $N_t \approx 10^{12}\ cm^{-3}$.

In full agreement with the experimental data, the TAT breakdown is not observed even at relatively high reverse biases, owing to compensation between TAT and SRH currents in p-n-junctions. The band-to-band (BTB) tunnelling

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is irrelevant in the voltage range of interest, and it becomes a dominant current mechanism only in the breakdown region, which justifies not including the BTB processes in the balance equations. In photodiodes with the band-gap $E_g > 0.1$ eV the diffusion current considerably affects the zero resistance R_0. It was also shown numerically that for p^+–n and n^+–p MCT diodes with 'inverted' donor and acceptor concentrations the differential resistance of biased diodes is practically the same in the region where the TAT+SRH processes dominate, although at zero bias their resistances differ considerably owing to the difference in the mobility of electrons and heavy holes.

3. Properties of CCD silicon readouts

Silicon readouts with direct injection input circuits and CCD multiplexers to be used with n-p-photovoltaic multielement arrays were designed, manufactured and tested at T = 77–300 K. The silicon readouts, in which skimming and partitioning functions are performed, too, because of the need for large area diodes and long cutoff wavelength of λ_{co} = 12.2 μm, were manufactured by n-channel MOS technology with 1.2 μm design rules with buried or surface channel CCD registers [15,16]. The designed CCD readouts are driven by four- or two-phase clock pulses. The amount of charge, which can be stored in the readouts depends on the mode used.

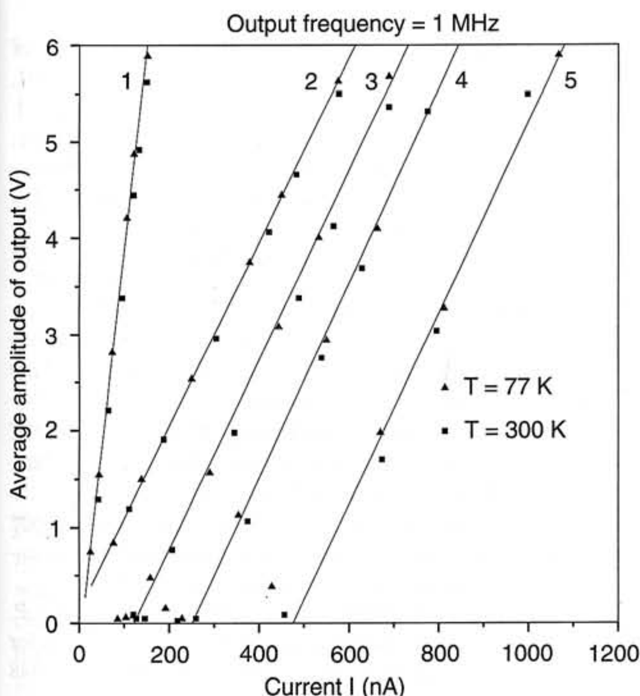

Fig. 6. Dependence of average amplitude of otput vs. input current for a silicon readout device without a photodiode linear array. 1 – mode without skimming and partition (τ = 16 μs): U_{c1} = 2.5 V, U_{c2} = 6.5 V, FPC = (1-1) V, FPS = (5-5) V. 2 – partition mode (τ = 8 s): U_{c1} = 5 V, U_{c2} = 5 V, FPC = (1-5) V, FPS = (0-5) V. 3, 4, 5 – skimming and partition mode (τ = 8 μs): U_{c2} = 5 V, FPS = (0-5) V and 3 – U_{c1} = 6 V, FPC = (1-6) V, 4 – U_{c1} = 7 V, FPC = (1-7) V, 5 – U_{c1} = 9 V, FPC = (1-9) V.

Without skimming and partitioning modes, it is 2.4 pC per channel at an output signal of 5 V. With a partitioning mode included, it is about 4.8 pC, and it is about 7.0 pC with skimming and partitioning modes switched on.

Different operating modes depending on the application purposes can be selected, taking into account, among others, programmable integration time, needed operating regime, availability of skimming level and partitioning factor. Before hybridisation, CCD readouts chips were tested on wafer level at 300 K with the help of testing transistors incorporated into inputs of the input transistors.

In Fig. 6, the possibilities one of the silicon CCD readout circuits operating in different modes are presented. Currents from photodiodes were emulated by the input resistors with different resistance values. By such testing it was confirmed that the CCD readouts could operate at high input currents correctly.

4. Hybridisation and FPA properties

The HgCdTe arrays and Si CCD readouts were hybridised by In bumps technology. The FPA hybridisation was performed by cold welding under external pressure on indium bumps via MCT and CCD silicon chips [11]. The maximum limit of mechanical load is determined from the measured curves of plastic flow of indium bumps, taking into account their height and area. The pressure required for plastic flow of the indium bumps lies in the range of 0.3–0.9 kg/mm^2. Investigations of the influence of vertical pressure on n-p-junction parameters on the HgCdTe layers have shown that degradation processes begin at pressures greater than 1.5 kg/mm^2 [17]. Thus, for reliable welding of indium bumps with hybridised modules, a pressure of no more than 1.0 kg/mm^2 was used, and the yield of this operation reached 100%. The total height of In bumps was about 12–15 μm. The dark currents were the same as measured for HgCdTe arrays.

Figure 7 showns the results of measurements for sensitivity of all 128 linear array diodes. From this figure one can conclude that the uniformity of the signals and sensitivity from the diodes is about ±10%.

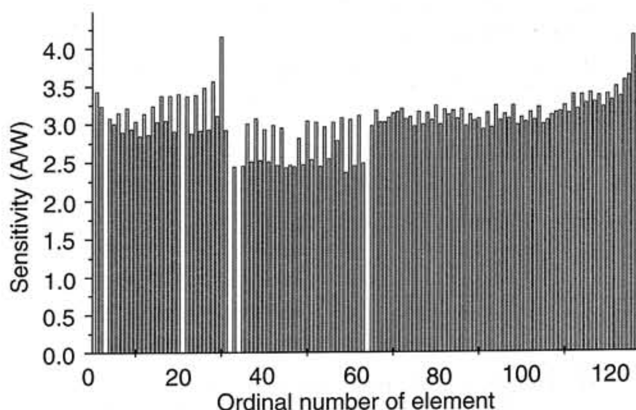

Fig. 7. Sensitivity of all FPA diodes.

Even with the skimming mode used for long integration times of 24–32 μs, needed in some cases for such large area n-p-junctions, the detectivity was near the ultimate performance limit for a given arrays. The dynamic range was not less than 60–65 dB, and the linearity transfer function was not valued at more than ±5%.

In Table 1, some performance parameters for one of 2×64 hybrid linear array of MBE grown MCT diodes with silicon CCD read-outs are presented.

Table 1. Some performance parameters for unquoted 2×64 hybrid linear array of MBE grown MCT diodes with silicon CCD read-outs.

Operating temperature (K)	80
Flat angle of view (deg)	40
Black body irradiance in the range of 1–13 μm (W/cm^2)	6×10^{-5}
Operating mode	Without skimming and partition
Integration time (μs)	8
Photodiode area (μm^2)	50×50
Dynamic range (dB)	≥ 65
Cut-off wavelength (μm)	12.2
NETD (without skimming and partition) (mK)	65
NETD (with skimming and partition) (mK)	25

5. Conclusions

HgCdTe layers were grown by MBE technology on (103) GaAs substrates with CdZnTe buffer layers, and silicon CCD read outs were manufactured according to traditional CCD technology. It was shown that electron concentration values observed in MCT layers can be explained by antisite non-equilibrium Te capture model during the MBE growth process. It was shown that the balance equation approach, taking into account TAT and SRH as two main current mechanisms, allows one to describe reasonably well the experimental data for MCT photodiodes in their operational voltage range. MCT LWIR linear arrays ($\lambda_{co} \approx 12.2$ μm) manufactured on MBE grown layers with large square diodes and CCD silicon readouts can operate close to BLIP regime.

Acknowledgements

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